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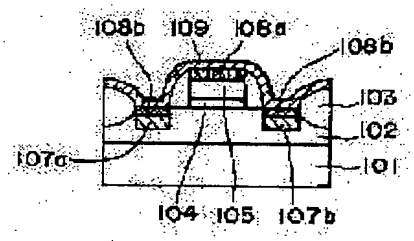
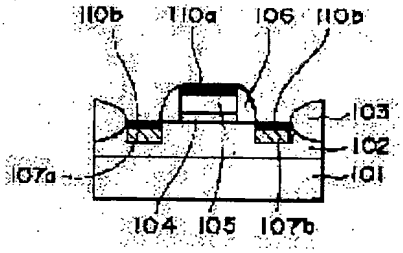
(54) SEMICONDUCTOR DEVICE HAVING MOS ELEMENTS AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device and a manufacturing method thereof, having a low resistance metal silicide layer obtained from a MOS structure having a gate electrode and a metal silicide layer on the source/drain region, without increasing the production man-hours and suppressed junction leak current.
SOLUTION: A p-type well diffused layer 102 is formed in a S substrate 10, element-isolated regions 103 are formed on the substrate, gate electrodes 105 of a Si-contained conductive layer and side wall spacers 106 are formed through an insulation film 104. An n-type impurity is diffused in the diffused layer 102 to form source/drain regions 107a, 107b. Ions of Ar or Kr not functioning as a dopant are implanted on the surfaces of the conductive layer 104 and diffused layer 107 to crystallize these surfaces. A Ti, Ni or other high- m. p. metal layer 109 is formed on the surface by the sputtering and heat treated to silicidize the metal layer, thus obtaining a desired semiconductor device.





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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The gate electrode which consists of a conductive layer which is formed through an insulator layer on a semi-conductor substrate, and contains silicon at least, And it is formed into said semi-conductor substrate, and has the impurity diffused layer which constitutes a source field or a drain field. Said gate electrode and said impurity diffused layer contain the MOS device which has a metal silicide layer on a front face. And said impurity diffused layer The semiconductor device containing a MOS device containing the atom which does not function as the donor or acceptor introduced by the ion implantation other than the impurity used as a donor or an acceptor.
[Claim 2] The atom which does not function as said donor or an acceptor in claim 1 is a semiconductor device containing a MOS device which is at least one sort chosen from at least one sort or the silicon, the germanium, carbon, and tin of the rare gas chosen from an argon, a krypton, neon, helium, and a xenon.
[Claim 3] The semiconductor device containing a MOS device with which the crystal defect formed in claims 1 or 2 with the atom which does not function as said donor or an acceptor, or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment exists in said impurity diffused layer.
[Claim 4] The gate electrode which consists of a conductive layer which is formed through an insulator layer on a semi-conductor substrate, and contains silicon at least, And it is formed into said semi-conductor substrate, and has the impurity diffused layer which constitutes a source field or a drain field. And said gate electrode and impurity diffused layer are the manufacture approach of the semiconductor device containing the MOS device which has a metal silicide layer on a front face, and mind an insulator layer on the (A) aforementioned semi-conductor substrate. The process which forms the conductive layer which contains silicon at least, and the impurity which serves as a donor or an acceptor into the (B) aforementioned semi-conductor substrate are diffused. The process which forms the impurity diffused layer which constitutes a source field or a drain field, (C) by performing the process which forms at least the metal layer which can form silicide in the front face of said conductive layer and said impurity diffused layer, and (D) heat treatment The process which silicide-izes said metal layer is included. Before the process (C) which forms said metal layer The manufacture approach including the process which pours in at least the atom which does not function on said conductive layer and said impurity diffused layer as a donor or an acceptor by the ion implantation of the semiconductor device containing a MOS device.
[Claim 5] The atom which does not function as said donor or an acceptor in claim 4 is the manufacture approach of the semiconductor device containing a MOS device which is at least one sort chosen from at least one sort or the silicon, the germanium, carbon, and tin of the rare gas chosen from an argon, a krypton, neon, helium, and a xenon.
[Claim 6] The manufacture approach of the semiconductor device containing a MOS device with which the crystal defect formed in claims 4 or 5 with the atom which does not function as said donor or an acceptor, or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment exists in said impurity diffused layer.

[Claim 7] Said ion implantation is the manufacture approach of the semiconductor device containing a MOS device performed [in / on either of claims 4-6, and / the MOS device of an N channel and a P channel] to coincidence.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device with which the front face of the MOS device formed by the Salicide technique, i.e., a gate electrode, the source / drain field contains the MOS device constituted by the metal silicide layer, and its manufacture approach.
[0002]
[A background technique and Object of the Invention] In recent years, the further high integration of a semiconductor integrated circuit and high performance-ization are aimed at, and detailed-izing of the component dimension of a device is being enhanced. Therefore, it is the situation which the width of face of the impurity diffused layer which constitutes the source / drain field of an MOS transistor (a source field or drain field) with detailed-izing also cannot but become narrow, and also cannot but make the depth shallow. However, the sheet resistance of an impurity diffused layer goes up, and it becomes impossible to disregard it to channel resistance of a transistor consequently, and it makes the engine performance of a semiconductor integrated circuit fall in respect of delay etc. as the depth of the source / drain field becomes shallow.
[0003] As opposed to such a problem, it is reference.;
Institute of telecommunications engineers Editing: An LSI handbook, Ohm-Sha As it is in p401, the Salicide (salicide:self-aligned-silicide) technique which silicide-izes the front face of the gate electrode which consists of the source / a drain field, and polycrystalline silicon by self-alignment is useful. By using the Salicide technique, it becomes possible to achieve low resistance-ization of the source / drain field demanded with detailed-izing.
[0004] However, reference;
(1) Robert Beyers et.al.J.Appl.Phys.61 (11), 1987. As indicated by (2) Minoru Takahashi et.al.Ext.Abs.1993 SSDM and p458 grade For the high concentration impurity which exists in a gate electrode and the source / drain field, especially the arsenic used for an N-channel metal oxide semiconductor transistor Or a silicide-ized reaction is controlled for detailed-izing that the width of face of the source / drain field, and a gate electrode becomes thin, and it is known that sheet resistance will go up.
[0005] As the cure, before forming silicide, the approach of carrying out the ion implantation of the arsenic to each front face of the gate electrode which consists of the source / a drain field, and polycrystalline silicon, making silicon amorphous, and forming the silicide of low resistance is learned.
[0006] This kind of approach is reference.;
(1) Wakabayashi ** ** -- the Institute of Electronics, Information and Communication Engineers technical research report It is indicated by SDM94-173(2) I.Sakai et.al.Digest 1992 Symposium on VLSI Technlgy and p66 grade. In the technique indicated by these reference, after pouring in the impurity for making it a conductivity-type semi-conductor and being activated to the source / drain field, and the gate electrode of a transistor, in order to make amorphous the front face of the source / drain field, and a gate electrode, an arsenic is poured in, and the method of

forming a silicide layer after that is taken.
[0007] However, if according to the technique which was expressed previously and which drives in an arsenic for the purpose of amorphous-izing the ion implantation of the arsenic is carried out all over a semi-conductor substrate in order to perform amorphous-ization, said arsenic will become a counter dope to the impurity layer of the P type which boron diffused, and will reduce the concentration of the P type impurity of an impurity layer relatively. Moreover, in order to avoid it, it is necessary to perform patterning using a photoresist and to drive an arsenic only into an N type field. However, in this approach, the number of sheets of the photo mask used for patterning at the time of a routing counter and an ion implantation increases, and it leads to increase of wafer processing cost.
[0008] Then, this invention tends to solve such a technical problem and the place made into the purpose has it in offering the semiconductor device containing a MOS device with which the rise of the sheet resistance accompanying detailed-izing of the source / drain field, and a gate electrode was controlled, and its manufacture approach.
[0009]
[Means for Solving the Problem] The manufacture approach of a semiconductor device concerning this invention is formed through an insulator layer on a semi-conductor substrate. It is formed into the gate electrode which consists of a conductive layer which contains silicon at least, and said semi-conductor substrate. It has the impurity diffused layer which constitutes a source field or a drain field. Said gate electrode and said impurity diffused layer are the manufacture approach of the semiconductor device containing the MOS device which has a metal silicide layer on a front face, and mind an insulator layer on the (A) aforementioned semi-conductor substrate. The process which forms the conductive layer which contains silicon at least, and the impurity which serves as a donor or an acceptor into the (B) aforementioned semi-conductor substrate are diffused. The process which forms the impurity diffused layer which constitutes a source field or a drain field, (C) by performing the process which forms at least the metal layer which can form silicide in the front face of said conductive layer and said impurity diffused layer, and (D) heat treatment The process which silicide-izes said metal layer is included. The process which pours in at least the atom which does not function on said conductive layer and said impurity diffused layer as a donor or an acceptor by the ion implantation before the process (C) which forms said metal layer is included.
[0010] The semiconductor device of this invention manufactured by the manufacture approach of this invention The gate electrode which consists of a conductive layer which is formed through an insulator layer on a substrate and contains silicon at least, And it is formed into said semi-conductor substrate, and has the impurity diffused layer which constitutes a source field or a drain field. And said impurity diffused layer contains the atom which does not function as the donor or acceptor introduced by the ion implantation other than the impurity used as a donor or an acceptor including the MOS device to which said gate electrode and said impurity diffused layer have a metal silicide layer on a front face.
[0011] The semiconductor device of this invention namely, before the process (C) which forms the metal layer which can form silicide by the manufacture approach of this invention The specific atomic ion which does not function on each front face of the conductive layer which constitutes the gate electrode of a MOS device, and the impurity diffused layer which constitutes the source / drain field as a donor or an acceptor is poured in by the ion implantation. By making amorphous each front face of said conductive layer and an impurity diffused layer, the reactivity of the silicon which constitutes said each class can be raised, and silicide-ization can be ensured. Therefore, a good metal silicide layer can be obtained, without affecting high impurity concentration, since it does not become a counter dope to the impurity of the both sides of N type and P type while controlling the rise of the sheet resistance of a metal silicide layer, when the width of face of a gate electrode and an impurity diffused layer becomes thin with detailed-izing of a component, and when the depth of said impurity diffused layer becomes small.
[0012] In the semiconductor device concerning this invention, and its manufacture approach, the atom which does not function as said donor or an acceptor has the desirable thing which is

chosen from at least one sort or the silicon, the germanium, carbon, and tin of the rare gas chosen from an argon, a krypton, neon, helium, and a xenon and which is an argon preferably at least one sort.

[0013] Since these atoms do not function as a donor or an acceptor, the concentration of the donor or acceptor contained to the source / drain field is not affected. Moreover, since these atoms have moderate mass, they can make the silicon of a processed layer amorphous efficiently and certainly by the ion implantation. Moreover, in the semiconductor device and its manufacture approach of this invention, it is desirable for the crystal defect formed with the atom which does not function as said donor or an acceptor, or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment to exist in said impurity diffused layer, namely, not to exceed outside the impurity diffused layer from which said crystal defect constitutes the source / drain field. Consequently, it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to an impurity diffused layer and a well] aiming at amorphous-izing is not performed.

[0014] For that purpose, it is desirable for the crystal defect which produces the acceleration energy at the time of the ion implantation aiming at amorphous-izing by the atomic ion which does not function as a donor or acceptors, such as argon ion, by the ion implantation, or the crystal defect formed at the process recovered by heat treatment of consecutiveness of the crystal defect to make it conditions which do not exceed the depth of the impurity diffused layer of the source / drain field of a MOS device.

[0015] Moreover, since according to the manufacture approach of this invention the specific atom introduced by the ion implantation for amorphous-izing does not change the high impurity concentration of the impurity diffused layer of the source / drain field as mentioned above, in manufacture of the semiconductor device containing an N channel and the MOS device of a P channel mold, said ion implantation can be performed to coincidence in the MOS device of N type and P type. Therefore, the mask formation process for avoiding a counter dope is not needed, but the ion implantation of the atomic ion which does not function as a donor or an acceptor can be performed all over a wafer.

[0016] as state above, it be in the condition did not become a counter dope to the impurity of the P type contain to the source / drain field, or N type, therefore a condition controlled the concentration of said impurity correctly, and, according to the semiconductor device and its manufacture approach of this invention, silicide-izing with a good impurity diffused layer be possible by perform amorphous-ization of silicon by the ion implantation of the atomic ion which do not function as a donor or acceptors, such as an argon ion.

[0017] Moreover, by performing amorphous-ization of silicon by the ion implantation of the atomic ion which does not function as a donor or an acceptor Since it does not become a counter dope to the impurity of the P type contained to the source / drain field, or N type Since it becomes possible to make amorphous each front face of the single-crystal-silicon layer which is the polycrystalline silicon layer, and the source / drain field which is a gate electrode by carrying out an ion implantation to coincidence on the whole wafer surface, It is not necessary to add a photograph process and to have good control of striking ion in any direction, and it becomes possible to reduce wafer processing cost.

[0018] When the semiconductor device of this invention is especially used for the product of a dc-battery power-source drive like a pocket device, for example, a cellular phone, a notebook computer, an electronic notebook, a pager, and a pocket game, while reducing the sheet resistance of a MOS device, junction leakage current can be controlled, therefore the current at the time of standby can be made small, and it enables prolongation-of-life-ization of a battery life to measure.

[0019]

[Embodiment of the Invention] Hereafter, the gestalt of typical operation of this invention is explained more to a detail, referring to a drawing.

[0020] (Gestalt of the 1st operation) The sectional view in which drawing 5 shows an example of the semiconductor device of this invention typically, drawing 1 - drawing 4 are the sectional views showing typically an example of the manufacture approach of the semiconductor device

shown in drawing 5 in order of a process.
[0021] The gestalt of this operation shows the example which applied this invention to the semiconductor device containing an N-channel metal oxide semiconductor component.
[0022] The semiconductor device shown in drawing 5 Gate oxide 104 is minded on a diffusion layer 102, the component isolation region 103 formed on said silicon substrate, and said silicon substrate 101. the P type formed in a silicon substrate 101 and this substrate 101 -- a well -- the formed gate electrode 105, the sidewall spacer 106 formed in both the sides of this gate electrode 105, and said well -- it is constituted including the source / drain fields 107a and 107b containing the N type impurity formed into the diffusion layer 102.
[0023] And N type impurities, such as Lynn, are doped by polycrystalline silicon, said gate electrode 105 is formed in it, and 1st metal silicide layer 110a is further formed in the front face of this gate electrode 105. Moreover, 2nd metal silicide layer 110b is formed in the front face of said source / drain fields 107a and 107b.
[0024] Furthermore, the atom which does not function as the donor or acceptor introduced by the ion implantation, for example, an argon, exists in said 1st and 2nd metal silicide layers 110a and 110b. Although this atom is explained in full detail behind, in order to promote silicide-ization, the atom doped by said gate electrode 105, and the source / drain fields 107a and 107b by the ion implantation remains.
[0025] The semiconductor device shown in drawing 5 can be manufactured according to the following processes shown in drawing 1 - drawing 4 .
[0026] (1) Form the 1st silicon oxide in an oxygen ambient atmosphere on a silicon substrate 101 first. next, a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. subsequently, the thermal diffusion method after pouring in boron using ion-implantation and removing said photoresist -- using -- P type -- a well -- a diffusion layer 102 is formed. Then, after forming a silicon nitride with a CVD method, a photoresist is applied, patterning of said photoresist is carried out, and only the part which forms a component isolation region in said 1st silicon oxide removes said silicon nitride in dry etching. Next, after removing said photoresist, the component isolation region 103 which consists of silicon oxide by making a mask oxidize said silicon nitride thermally in an oxygen ambient atmosphere is formed.
[0027] Subsequently, a phosphoric acid etc. removes said silicon nitride, it oxidizes thermally further for the impurity removal on the front face of a substrate before formation of gate oxide, and the 2nd silicon oxide is formed. Then, after etching removes said 2nd silicon oxide, gate oxide 104 is formed using the oxidizing [thermally] method. Next, a polycrystalline silicon layer is formed using a CVD method, after applying and carrying out patterning of the photoresist, dry etching is performed, the gate electrode 105 is formed, and said photoresist is removed (drawing 1).
[0028] (2) Next, perform dry etching and form the sidewall spacer 106, after using a CVD method and forming an oxide film, in order to prevent the short-circuit between the gate electrode-source / drain field after silicide. Next, in order to pour in formation of the source / drain field of an N-channel metal oxide semiconductor transistor, and the impurity to the inside of the gate electrode 105, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms an N-channel metal oxide semiconductor transistor. Next, while pouring in N type impurities, such as an arsenic, with ion-implantation and forming the source / drain fields 107a and 107b which are high-concentration N type diffusion layers, respectively, an impurity is introduced into said gate electrode 105, and said photoresist is removed after that. Next, in order to activate the poured-in impurity, it heat-treats in nitrogen-gas-atmosphere mind (drawing 2).
[0029] (3) Next, after removing the natural oxidation film which exists in each front face of the gate electrode 105, and the source / drain fields 107a and 107b, in order to make amorphous each front face of the gate electrode 105, and the source / drain fields 107a and 107b, pour in argon ion. The depth of the source / drain fields 107a and 107b of the acceleration energy at this time is 0.2 micrometers. In the case so that heat treatment for 20 minutes may be performed at 800-900 degrees C after an argon ion implantation 15 or less keVs are desirable so

that the crystal defect formed with the poured-in argon ion or the crystal defect in which the crystal defect is formed in the process recovered by consecutive heat treatment may not exceed the depth of the source / drain fields 107a and 107b. Thus, the amorphous fields 108a and 108b are formed in each front face of the gate electrode 105, and the source / drain fields 107a and 107b (drawing 3).

[0030] It is important by carrying out the ion implantation of the specific ion, such as argon ion, to each front face of said gate electrode 105, and the source / drain fields 107a and 107b at this process to promote amorphous-ization of silicon. However, it is desirable to make it the crystal defect formed with said specific atomic ion, such as the crystal defect which crosses the source / drain field by this ion implantation, i.e., an argon etc., or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment not exceed outside said source / drain fields 107a and 107b. consequently, the source / drain field, and a well -- it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to a diffusion layer] aiming at amorphous-izing is not performed. For that purpose, it is desirable to set the acceleration energy at the time of the ion implantation by the atomic ion which does not function as a donor or acceptors, such as argon ion, as conditions on which said crystal defect does not exceed the depth of the impurity diffused layer of the source / drain field.

[0031] (4) Next, form the metal layer 109 which consists of the metal layer which can form silicide using a spatter, for example, titanium, cobalt, nickel, a tantalum, platinum, or these alloys (drawing 4), heat-treat using lamp ANIRA, such as halogen lamp ANIRA, after that, and form the metal silicide layers 110a and 110b in the front face of the gate electrode 105, and the source / drain fields 107a and 107b by self-alignment. Subsequently, selectivity etching is performed and the unreacted metal layer on the sidewall spacer 106 and the component isolation region 103 is removed (drawing 5).

[0032] As stated above, it sets to the manufacture approach of this invention. On each front face of the source / drain fields 107a and 107b which consists of a gate electrode 105 which consists of polycrystalline silicon before the process (4) which forms the metal layer which can form silicide, and an N type impurity diffused layer By pouring in the specific atomic ion which does not function as a donor or an acceptor by the ion implantation, and having the process (3) which makes said each front face amorphous The reactivity of the silicon which constitutes each class of said gate electrode 105, and the source / drain fields 107a and 107b which consist of an N type impurity diffused layer can be raised, and silicide-ization can be ensured. Therefore, when the width of face of a gate electrode and the source / drain field becomes thin with detailed-izing of a component, and when the depth of said source / drain field becomes small, it also sets. A good metal silicide layer can be obtained without affecting high impurity concentration in the source / drain field containing an N type impurity, especially the arsenic which is easy to check silicide-ization, while controlling the rise of the sheet resistance of a metal silicide layer. Moreover, since the ion kind to pour in is the argon which is not the impurity of an arsenic, N type, such as Lynn and BF2, or P type, it does not become a counter dope to other impurities.

[0033] In addition, in the gestalt of the above-mentioned implementation, although N-channel metal oxide semiconductor tolan JISHITA was described, it cannot be overemphasized that this invention can be applied similarly and can attain the same function also about a P channel MOS transistor if the point that a conductivity type is mainly reversed polarity is removed.

[0034] Next, the example of an experiment performed in relation to the MOS device concerning the gestalt of this operation is explained.

[0035] (Example of an experiment)

(1) The sample was formed according to the process which carried out the SIMS above-mentioned, and it asked for the profile of each atom of the direction of thickness of a sample according to the secondary ion mass spectrometry (SIMS) by the exposure of primary caesium ion. The result is shown in drawing 6 . As for the sample used for measurement, the polycrystalline silicon layer (220nm) the silicon oxide (10nm) which is gate oxide, acceleration energy 50keV, and 4x1015 doses /are [cm] 2, and are [layer] the gate electrode with which the arsenic was doped, and a titanium silicide layer (70-80nm) are formed on a silicon substrate.

And in case this sample is formed, argon ion is poured in with the acceleration energy of 10keV (s) by said process (3).

[0036] It was checked that the peak of an argon is in its layer near the front face of the titanium silicide layer which is the maximum upper layer from drawing 6 .

[0037] (2) The line breadth dependency of the sheet resistance of a gate electrode which the existence of impregnation of argon ion exerts on effect drawing 7 which impregnation of argon ion exerts on the sheet resistance of a gate electrode is compared and shown. In drawing 7 , an axis of abscissa shows the line breadth of the metal silicide layer of a gate electrode, and an axis of ordinate shows the sheet resistance of the gate electrode of electrical-potential-difference 3.3V. Moreover, the sample concerning this invention has the same configuration fundamentally with having used by measurement of the above (1), and two or more sorts of things from which the line breadth of a titanium silicide layer differs were used for it. The sample for a comparison is the same as that of what there is no impregnation of argon ion, and also starts this invention.

[0038] From drawing 7 , by performing amorphous-ization of a gate electrode surface by the ion implantation using argon ion shows that sheet resistance is remarkably small in the range where the line breadth of the titanium silicide layer of a gate electrode is wide compared with the case where argon ion is not poured in. Moreover, when the line breadth of the titanium silicide layer of a gate electrode became small, it was checked that the effectiveness of suppressing the rise of sheet resistance is large.

[0039] (3) The line breadth dependency of the sheet resistance of the source / drain field which the existence of impregnation of argon ion exerts on effect drawing 8 which impregnation of argon ion exerts on the sheet resistance of the source / drain field is compared and shown. In drawing 8 , an axis of abscissa shows the line breadth of the titanium silicide layer of the source / drain field, and an axis of ordinate shows the sheet resistance of the source / drain field of electrical-potential-difference 3.3V. Moreover, the sample concerning this invention has the same configuration fundamentally with what was used by measurement of the above (1), and two or more sorts of things from which the line breadth of a titanium silicide layer differs were used for it. Acceleration energy 50keV and 4x1015 doses /are [cm] 2, and, as for the source / drain field, an arsenic is doped.

[0040] From drawing 8 , by performing amorphous-ization of the source / drain field front face by the ion implantation using argon ion shows that sheet resistance is small in the range where the line breadth of the metal silicide layer of the source / drain field is wide compared with the case where argon ion is not poured in.

[0041] (4) The acceleration energy of argon ion shows the effect which it has on junction leakage current to effect drawing 9 which the acceleration energy of an ion implantation exerts on junction leakage current. In drawing 9 , an axis of abscissa shows the impregnation energy of argon ion, and an axis of ordinate shows the leakage current of electrical-potential-difference 3.3V. The sample used for measurement is the same as that of what was used by measurement of the above (3). Moreover, 41472 micrometers of area of the evaluated area are 2, and the circumference length of area is 864 micrometers.

[0042] the acceleration energy at drawing 9 to the time of an argon ion implantation -- when it becomes large, it turns out that junction leakage current also becomes large. Therefore, as for the acceleration energy at the time of an ion implantation, it is desirable to be set up so that junction leakage current may not exceed a predetermined value. That is, since it is thought that junction leakage current increases when the crystal defect produced by the ion implantation or the defect in which the crystal defect is formed in the process recovered by consecutive heat treatment crosses the source / drain field, as for the acceleration energy at the time of an ion implantation, it is desirable to be set up so that these crystal defects may not cross the source / drain field.

[0043] For example, as shown in drawing 9 , it is possible by setting the acceleration energy at the time of an ion implantation as the suitable range (15 or less keVs) to hold down to the leakage current of the case where argon ion is not being poured in, and this level. However, since the optimum value changes with components, acceleration energy cannot generally limit the value.

[0044] (5) A crystal defect shows the effect which it has on junction leakage current to effect drawing 10 which a crystal defect exerts on junction leakage current. In drawing 10 , an axis of abscissa shows the thermal wave signal for which it asked by the thermal waving method, and an axis of ordinate shows the junction leak current value of electrical-potential-difference 3.3V. According to the thermal waving method, the quantum of the damage generated in the silicon substrate can be carried out indirectly, and the crystal defect in silicon can be evaluated. The sample of a fundamental configuration used for measurement is the same as that of what was used for measurement of the above (4), and drives it in on the conditions which change an argon with ion implantations. The placing conditions of an argon are as follows.
[0045] a. Dose; the same sign shows [in / 3x1014 pieces // 2, acceleration energy;10keVb. dose;1x1015 piece/cm2, acceleration energy;10keVc. dose;3x1014 piece/cm2, and acceleration energy;30keV drawing 10] the thing corresponding to the placing conditions of the above-mentioned argon cm. In addition, the thermal wave signal shown in the axis of abscissa of drawing 10 measures not using the sample which measured junction leakage current but using the sample which carried out the ion implantation of the argon on above-mentioned a-c and the same conditions at BEASHIRIKON. Moreover, 250000 micrometers of area of the area which evaluated junction leakage current are 2, and the circumference length of area is 2000 micrometers.
[0046] Drawing 10 shows that junction leakage current becomes large as the value of a thermal wave signal becomes large. It shows that junction leakage current becomes large as the crystal defect of this increases.
[0047] (Gestalt of the 2nd operation) Drawing 14 is the sectional view which applied this invention to the CMOS device and in which showing the gestalt of other operations typically, and drawing 11 - drawing 13 are the sectional views showing typically the production process of the semiconductor device shown in drawing 14 .
[0048] The semiconductor device shown in drawing 14 can be manufactured according to the following processes shown in drawing 1111 - drawing 13 .
[0049] (1) Form a twin well by the approach usually used first. That is, the 1st silicon oxide is formed in an oxygen ambient atmosphere on a silicon substrate 101. next, a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. Subsequently, Lynn is poured in using ion-implantation and said photoresist is removed. next, P type -- a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. Subsequently, boron is poured in instead of Lynn using ion-implantation, and said photoresist is removed. then, a thermal diffusion method -- using -- N type -- a well -- diffusion layer 102b and P type -- a well -- diffusion layer 102a is formed.
[0050] Subsequently, after forming a silicon nitride with a CVD method on the 1st silicon oxide, a photoresist is applied, patterning of said photoresist is carried out, and only the part which forms a component isolation region in said 1st silicon oxide removes said silicon nitride in dry etching. Next, after removing said photoresist, the component isolation region 103 which consists of silicon oxide by making a mask oxidize said silicon nitride thermally in an oxygen ambient atmosphere is formed.
[0051] Subsequently, a phosphoric acid etc. removes said silicon nitride, it oxidizes thermally further for the impurity removal on the front face of a substrate before formation of gate oxide, and the 2nd silicon oxide is formed. Then, after etching removes said 2nd silicon oxide, gate oxide 104a and 104b is formed using the oxidizing [thermally] method. Next, a polycrystalline silicon layer is formed using a CVD method, after applying and carrying out patterning of the photoresist, dry etching is performed, gate electrode 105a of an N-channel metal oxide semiconductor transistor and gate electrode 105b of a P channel MOS transistor are formed, and said photoresist is removed.
[0052] Next, in order to carry out short prevention between the gate electrode-source / drain field after silicide, after using a CVD method and forming an oxide film, dry etching is performed and the sidewall spacer 106 is formed. Next, in order to pour in formation of the source / drain field of an N-channel metal oxide semiconductor transistor, and the impurity to the inside of gate

electrode 105a, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms an N-channel metal oxide semiconductor transistor. Next, while pouring in N type impurities, such as an arsenic, with ion-implantation and forming the source / drain fields 107a and 107b which are high-concentration N type diffusion layers, respectively, an impurity is introduced into said gate electrode 105a, and said photoresist is removed after that.

[0053] Similarly, in order to pour in formation of the source / drain field of a P channel MOS transistor, and the impurity to the inside of gate electrode 105b, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms a P channel MOS transistor. Next, while pouring in P type impurities, such as boron, with ion-implantation and forming the source / drain fields 107c and 107d which are high-concentration P type diffusion layers, respectively, an impurity is introduced into said gate electrode 105b, and said photoresist is removed after that. Next, in order to activate the poured-in impurity, it heat-treats in nitrogen-gas-atmosphere mind (drawing 11 R> 1).

[0054] (2) Next, after removing the natural oxidation film which exists in each the gate electrodes 105a and 105b (105), and fields [the source / drain fields / 107a, 107b, 107c, and 107d (107)] front face, in order to make amorphous each front face of said gate electrode 105, and the source / drain field 107, pour in argon ion. The acceleration energy at this time has 15 or less desirable keVs so that the depth of the source / drain field 107 is 0.2 micrometers, and the crystal defect formed with the poured-in argon ion or the crystal defect in which that crystal defect is formed in the process recovered by consecutive heat treatment may not exceed the depth of the source / drain field 107, when performing heat treatment for 20 minutes at 800-900 degrees C after an argon ion implantation. Thus, the amorphous fields 108a and 108c are formed in each front face of the gate electrodes 105a and 105b, and the amorphous fields 108b and 108d are formed in each the source / drain fields 107a and 107b of N-channel metal oxide semiconductor tolan JISHITA, and fields [of P channel MOS tolan JISHITA / the source / drain fields / 107c and 107d] front face (drawing 12 R> 2).

[0055] As mentioned above at this process, it is important for each front face of said gate electrode 105, and the source / drain field 107 by carrying out the ion implantation of the specific ion, such as argon ion, to promote amorphous-ization of silicon. However, it is desirable to make it the crystal defect formed with said specific atomic ion, such as the crystal defect which crosses the source / drain field 107 by this ion implantation, i.e., an argon etc., or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment not exceed outside said source / drain field 107. consequently, the source / drain field, and a well -- it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to a diffusion layer] aiming at amorphous-izing is not performed. For that purpose, it is desirable to set the acceleration energy at the time of the ion implantation by the atomic ion which does not function as a donor or acceptors, such as argon ion, as conditions on which said crystal defect does not exceed the depth of the impurity diffused layer of the source / drain field.

[0056] And a mask formation process to avoid [for that it is characteristic at this process to be able to perform an ion implantation with a blanket to coincidence, i.e., the whole wafer surface, to the MOS transistor of an N channel and a P channel, since the atomic ion which does not function as a donor or an acceptor, for example, argon ion, is used for the ion implantation for amorphous-izing and] a counter dope is not needed, but it becomes possible to reduce wafer processing cost.

[0057] (3) Next, the metal layer which can form silicide using a spatter, for example, titanium, cobalt, nickel, a tantalum, or platinum, Or form the metal layer 109 which consists of these alloys (drawing 13), and it heat-treats using lamp ANIRA. The metal silicide layers 110a and 110c are formed in each front face of the gate electrodes 105a and 105b. The metal silicide layers 110b and 110d are formed in each the source / drain fields 107a and 107b of N-channel metal oxide semiconductor tolan JISHITA, and fields [of P channel MOS tolan JISHITA / the source / drain fields / 107c and 107d] front face by self-alignment. Subsequently, selectivity etching is performed and the unreacted metal layer on the sidewall spacer 106 and the component isolation

region 103 is removed (drawing 14 R> 4).
[0058] As stated above, it also sets in the gestalt of this operation. Like the gestalt of said operation On each fields [which consist of the gate electrode 105 which consists of polycrystalline silicon before the process (3) which forms the metal layer which can form silicide and N type, or a P type impurity diffused layer / the source / drain fields 107a, 107b, 107c, and 107d] front face By pouring in the specific atomic ion which does not function as a donor or an acceptor by the ion implantation, and having the process (2) which makes said each front face amorphous The reactivity of the silicon which constitutes the source / drain fields 107a, 107b, 107c, and 107d which consist of said gate electrode 105 and N type, or a P type impurity diffused layer can be raised, and silicide-ization can be ensured. Therefore, a good metal silicide layer can be obtained, without affecting the concentration of the impurity of the N type contained to the source / drain field, or P type, while controlling the rise of the sheet resistance of a metal silicide layer, when the width of face of a gate electrode and an impurity diffused layer becomes thin with detailed-izing of a component, and when the depth of said source / drain field becomes small. Moreover, since the ion kind to pour in is the argon which is not the impurity of an arsenic, N type, such as Lynn and BF2, or P type, it does not become a counter dope to the impurity of N type or P type.
[0059] As mentioned above, although this invention was explained based on the gestalt of operation, it cannot be overemphasized that modification various in the range which does not deviate from the summary is possible for this invention, without being limited to the gestalt of the above-mentioned implementation.
[0060]

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor device with which the front face of the MOS device formed by the Salicide technique, i.e., a gate electrode, the source / drain field contains the MOS device constituted by the metal silicide layer, and its manufacture approach.

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TECHNICAL PROBLEM

[A background technique and Object of the Invention] In recent years, the further high integration of a semiconductor integrated circuit and high performance-ization are aimed at, and detailed-izing of the component dimension of a device is being enhanced. Therefore, it is the situation which the width of face of the impurity diffused layer which constitutes the source / drain field of an MOS transistor (a source field or drain field) with detailed-izing also cannot but become narrow, and also cannot but make the depth shallow. However, the sheet resistance of an impurity diffused layer goes up, and it becomes impossible to disregard it to channel resistance of a transistor consequently, and it makes the engine performance of a semiconductor integrated circuit fall in respect of delay etc. as the depth of the source / drain field becomes shallow.
[0003] As opposed to such a problem, it is reference.;
Institute of telecommunications engineers Editing: An LSI handbook, Ohm-Sha As it is in p401, the Salicide (salicide:self-aligned-silicide) technique which silicide-izes the front face of the gate electrode which consists of the source / a drain field, and polycrystalline silicon by self-alignment is useful. By using the Salicide technique, it becomes possible to achieve low resistance-ization of the source / drain field demanded with detailed-izing.
[0004] However, reference;
(1) Robert Beyers et.al.J.Appl.Phys.61 (11), 1987. As indicated by (2) Minoru Takahashi et.al.Ext.Abs.1993 SSDM and p458 grade For the high concentration impurity which exists in a gate electrode and the source / drain field, especially the arsenic used for an N-channel metal oxide semiconductor transistor Or a silicide-ized reaction is controlled for detailed-izing that the width of face of the source / drain field, and a gate electrode becomes thin, and it is known that sheet resistance will go up.
[0005] As the cure, before forming silicide, the approach of carrying out the ion implantation of the arsenic to each front face of the gate electrode which consists of the source / a drain field, and polycrystalline silicon, making silicon amorphous, and forming the silicide of low resistance is learned.
[0006] This kind of approach is reference.;
(1) Wakabayashi ** ** -- the Institute of Electronics, Information and Communication Engineers technical research report It is indicated by SDM94-173(2) I.Sakai et.al.Digest 1992 Symposium on VLSI Technlgy and p66 grade. In the technique indicated by these reference, after pouring in the impurity for making it a conductivity-type semi-conductor and being activated to the source / drain field, and the gate electrode of a transistor, in order to make amorphous the front face of the source / drain field, and a gate electrode, an arsenic is poured in, and the method of forming a silicide layer after that is taken.
[0007] However, if according to the technique which was expressed previously and which drives in an arsenic for the purpose of amorphous-izing the ion implantation of the arsenic is carried out all over a semi-conductor substrate in order to perform amorphous-ization, said arsenic will become a counter dope to the impurity layer of the P type which boron diffused, and will reduce the concentration of the P type impurity of an impurity layer relatively. Moreover, in order to avoid it, it is necessary to perform patterning using a photoresist and to drive an arsenic only

into an N type field. However, in this approach, the number of sheets of the photo mask used for patterning at the time of a routing counter and an ion implantation increases, and it leads to increase of wafer processing cost.

[0008] Then, this invention tends to solve such a technical problem and the place made into the purpose has it in offering the semiconductor device containing a MOS device with which the rise of the sheet resistance accompanying detailed-izing of the source / drain field, and a gate electrode was controlled, and its manufacture approach.

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MEANS

[Means for Solving the Problem] The manufacture approach of a semiconductor device concerning this invention is formed through an insulator layer on a semi-conductor substrate. It is formed into the gate electrode which consists of a conductive layer which contains silicon at least, and said semi-conductor substrate. It has the impurity diffused layer which constitutes a source field or a drain field. Said gate electrode and said impurity diffused layer are the manufacture approach of the semiconductor device containing the MOS device which has a metal silicide layer on a front face, and mind an insulator layer on the (A) aforementioned semi-conductor substrate. The process which forms the conductive layer which contains silicon at least, and the impurity which serves as a donor or an acceptor into the (B) aforementioned semi-conductor substrate are diffused. The process which forms the impurity diffused layer which constitutes a source field or a drain field, (C) by performing the process which forms at least the metal layer which can form silicide in the front face of said conductive layer and said impurity diffused layer, and (D) heat treatment The process which silicide-izes said metal layer is included. The process which pours in at least the atom which does not function on said conductive layer and said impurity diffused layer as a donor or an acceptor by the ion implantation before the process (C) which forms said metal layer is included.
[0010] The semiconductor device of this invention manufactured by the manufacture approach of this invention The gate electrode which consists of a conductive layer which is formed through an insulator layer on a substrate and contains silicon at least, And it is formed into said semi-conductor substrate, and has the impurity diffused layer which constitutes a source field or a drain field. And said impurity diffused layer contains the atom which does not function as the donor or acceptor introduced by the ion implantation other than the impurity used as a donor or an acceptor including the MOS device to which said gate electrode and said impurity diffused layer have a metal silicide layer on a front face.
[0011] The semiconductor device of this invention namely, before the process (C) which forms the metal layer which can form silicide by the manufacture approach of this invention The specific atomic ion which does not function on each front face of the conductive layer which constitutes the gate electrode of a MOS device, and the impurity diffused layer which constitutes the source / drain field as a donor or an acceptor is poured in by the ion implantation. By making amorphous each front face of said conductive layer and an impurity diffused layer, the reactivity of the silicon which constitutes said each class can be raised, and silicide-ization can be ensured. Therefore, a good metal silicide layer can be obtained, without affecting high impurity concentration, since it does not become a counter dope to the impurity of the both sides of N type and P type while controlling the rise of the sheet resistance of a metal silicide layer, when the width of face of a gate electrode and an impurity diffused layer becomes thin with detailed-izing of a component, and when the depth of said impurity diffused layer becomes small.
[0012] In the semiconductor device concerning this invention, and its manufacture approach, the atom which does not function as said donor or an acceptor has the desirable thing which is chosen from at least one sort or the silicon, the germanium, carbon, and tin of the rare gas chosen from an argon, a krypton, neon, helium, and a xenon and which is an argon preferably at

least one sort.
[0013] Since these atoms do not function as a donor or an acceptor, the concentration of the donor or acceptor contained to the source / drain field is not affected. Moreover, since these atoms have moderate mass, they can make the silicon of a processed layer amorphous efficiently and certainly by the ion implantation. Moreover, in the semiconductor device and its manufacture approach of this invention, it is desirable for the crystal defect formed with the atom which does not function as said donor or an acceptor, or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment to exist in said impurity diffused layer, namely, not to exceed outside the impurity diffused layer from which said crystal defect constitutes the source / drain field. Consequently, it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to an impurity diffused layer and a well] aiming at amorphous-izing is not performed.
[0014] For that purpose, it is desirable for the crystal defect which produces the acceleration energy at the time of the ion implantation aiming at amorphous-izing by the atomic ion which does not function as a donor or acceptors, such as argon ion, by the ion implantation, or the crystal defect formed at the process recovered by heat treatment of consecutiveness of the crystal defect to make it conditions which do not exceed the depth of the impurity diffused layer of the source / drain field of a MOS device.
[0015] Moreover, since according to the manufacture approach of this invention the specific atom introduced by the ion implantation for amorphous-izing does not change the high impurity concentration of the impurity diffused layer of the source / drain field as mentioned above, in manufacture of the semiconductor device containing an N channel and the MOS device of a P channel mold, said ion implantation can be performed to coincidence in the MOS device of N type and P type. Therefore, the mask formation process for avoiding a counter dope is not needed, but the ion implantation of the atomic ion which does not function as a donor or an acceptor can be performed all over a wafer.
[0016] as state above, it be in the condition did not become a counter dope to the impurity of the P type contain to the source / drain field, or N type, therefore a condition controlled the concentration of said impurity correctly, and, according to the semiconductor device and its manufacture approach of this invention, silicide-izing with a good impurity diffused layer be possible by perform amorphous-ization of silicon by the ion implantation of the atomic ion which do not function as a donor or acceptors, such as an argon ion.
[0017] Moreover, by performing amorphous-ization of silicon by the ion implantation of the atomic ion which does not function as a donor or an acceptor Since it does not become a counter dope to the impurity of the P type contained to the source / drain field, or N type Since it becomes possible to make amorphous each front face of the single-crystal-silicon layer which is the polycrystalline silicon layer, and the source / drain field which is a gate electrode by carrying out an ion implantation to coincidence on the whole wafer surface, It is not necessary to add a photograph process and to have good control of striking ion in any direction, and it becomes possible to reduce wafer processing cost.
[0018] When the semiconductor device of this invention is especially used for the product of a dc-battery power-source drive like a pocket device, for example, a cellular phone, a notebook computer, an electronic notebook, a pager, and a pocket game, while reducing the sheet resistance of a MOS device, junction leakage current can be controlled, therefore the current at the time of standby can be made small, and it enables prolongation-of-life-ization of a battery life to measure.
[0019]
[Embodiment of the Invention] Hereafter, the gestalt of typical operation of this invention is explained more to a detail, referring to a drawing.
[0020] (Gestalt of the 1st operation) The sectional view in which drawing 5 shows an example of the semiconductor device of this invention typically, drawing 1 - drawing 4 are the sectional views showing typically an example of the manufacture approach of the semiconductor device shown in drawing 5 in order of a process.
[0021] The gestalt of this operation shows the example which applied this invention to the

semiconductor device containing an N-channel metal oxide semiconductor component.
[0022] The semiconductor device shown in drawing 5 Gate oxide 104 is minded on a diffusion layer 102, the component isolation region 103 formed on said silicon substrate, and said silicon substrate 101. the P type formed in a silicon substrate 101 and this substrate 101 -- a well -- the formed gate electrode 105, the sidewall spacer 106 formed in both the sides of this gate electrode 105, and said well -- it is constituted including the source / drain fields 107a and 107b containing the N type impurity formed into the diffusion layer 102.
[0023] And N type impurities, such as Lynn, are doped by polycrystalline silicon, said gate electrode 105 is formed in it, and 1st metal silicide layer 110a is further formed in the front face of this gate electrode 105. Moreover, 2nd metal silicide layer 110b is formed in the front face of said source / drain fields 107a and 107b.
[0024] Furthermore, the atom which does not function as the donor or acceptor introduced by the ion implantation, for example, an argon, exists in said 1st and 2nd metal silicide layers 110a and 110b. Although this atom is explained in full detail behind, in order to promote silicide-ization, the atom doped by said gate electrode 105, and the source / drain fields 107a and 107b by the ion implantation remains.
[0025] The semiconductor device shown in drawing 5 can be manufactured according to the following processes shown in drawing 1 - drawing 4 .
[0026] (1) Form the 1st silicon oxide in an oxygen ambient atmosphere on a silicon substrate 101 first. next, a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. subsequently, the thermal diffusion method after pouring in boron using ion-implantation and removing said photoresist -- using -- P type -- a well -- a diffusion layer 102 is formed. Then, after forming a silicon nitride with a CVD method, a photoresist is applied, patterning of said photoresist is carried out, and only the part which forms a component isolation region in said 1st silicon oxide removes said silicon nitride in dry etching. Next, after removing said photoresist, the component isolation region 103 which consists of silicon oxide by making a mask oxidize said silicon nitride thermally in an oxygen ambient atmosphere is formed.
[0027] Subsequently, a phosphoric acid etc. removes said silicon nitride, it oxidizes thermally further for the impurity removal on the front face of a substrate before formation of gate oxide, and the 2nd silicon oxide is formed. Then, after etching removes said 2nd silicon oxide, gate oxide 104 is formed using the oxidizing [thermally] method. Next, a polycrystalline silicon layer is formed using a CVD method, after applying and carrying out patterning of the photoresist, dry etching is performed, the gate electrode 105 is formed, and said photoresist is removed (drawing 1).
[0028] (2) Next, perform dry etching and form the sidewall spacer 106, after using a CVD method and forming an oxide film, in order to prevent the short-circuit between the gate electrode-source / drain field after silicide. Next, in order to pour in formation of the source / drain field of an N-channel metal oxide semiconductor transistor, and the impurity to the inside of the gate electrode 105, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms an N-channel metal oxide semiconductor transistor. Next, while pouring in N type impurities, such as an arsenic, with ion-implantation and forming the source / drain fields 107a and 107b which are high-concentration N type diffusion layers, respectively, an impurity is introduced into said gate electrode 105, and said photoresist is removed after that. Next, in order to activate the poured-in impurity, it heat-treats in nitrogen-gas-atmosphere mind (drawing 2).
[0029] (3) Next, after removing the natural oxidation film which exists in each front face of the gate electrode 105, and the source / drain fields 107a and 107b, in order to make amorphous each front face of the gate electrode 105, and the source / drain fields 107a and 107b, pour in argon ion. The depth of the source / drain fields 107a and 107b of the acceleration energy at this time is 0.2 micrometers. In the case so that heat treatment for 20 minutes may be performed at 800-900 degrees C after an argon ion implantation 15 or less keVs are desirable so that the crystal defect formed with the poured-in argon ion or the crystal defect in which the crystal defect is formed in the process recovered by consecutive heat treatment may not

exceed the depth of the source / drain fields 107a and 107b. Thus, the amorphous fields 108a and 108b are formed in each front face of the gate electrode 105, and the source / drain fields 107a and 107b (drawing 3).
[0030] It is important by carrying out the ion implantation of the specific ion, such as argon ion, to each front face of said gate electrode 105, and the source / drain fields 107a and 107b at this process to promote amorphous-ization of silicon. However, it is desirable to make it the crystal defect formed with said specific atomic ion, such as the crystal defect which crosses the source / drain field by this ion implantation, i.e., an argon etc., or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment not exceed outside said source / drain fields 107a and 107b. consequently, the source / drain field, and a well -- it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to a diffusion layer] aiming at amorphous-izing is not performed. For that purpose, it is desirable to set the acceleration energy at the time of the ion implantation by the atomic ion which does not function as a donor or acceptors, such as argon ion, as conditions on which said crystal defect does not exceed the depth of the impurity diffused layer of the source / drain field.
[0031] (4) Next, form the metal layer 109 which consists of the metal layer which can form silicide using a spatter, for example, titanium, cobalt, nickel, a tantalum, platinum, or these alloys (drawing 4), heat-treat using lamp ANIRA, such as halogen lamp ANIRA, after that, and form the metal silicide layers 110a and 110b in the front face of the gate electrode 105, and the source / drain fields 107a and 107b by self-alignment. Subsequently, selectivity etching is performed and the unreacted metal layer on the sidewall spacer 106 and the component isolation region 103 is removed (drawing 5).
[0032] As stated above, it sets to the manufacture approach of this invention. On each front face of the source / drain fields 107a and 107b which consists of a gate electrode 105 which consists of polycrystalline silicon before the process (4) which forms the metal layer which can form silicide, and an N type impurity diffused layer By pouring in the specific atomic ion which does not function as a donor or an acceptor by the ion implantation, and having the process (3) which makes said each front face amorphous The reactivity of the silicon which constitutes each class of said gate electrode 105, and the source / drain fields 107a and 107b which consist of an N type impurity diffused layer can be raised, and silicide-ization can be ensured. Therefore, when the width of face of a gate electrode and the source / drain field becomes thin with detailed-izing of a component, and when the depth of said source / drain field becomes small, it also sets. A good metal silicide layer can be obtained without affecting high impurity concentration in the source / drain field containing an N type impurity, especially the arsenic which is easy to check silicide-ization, while controlling the rise of the sheet resistance of a metal silicide layer. Moreover, since the ion kind to pour in is the argon which is not the impurity of an arsenic, N type, such as Lynn and BF2, or P type, it does not become a counter dope to other impurities.
[0033] In addition, in the gestalt of the above-mentioned implementation, although N-channel metal oxide semiconductor tolan JISHITA was described, it cannot be overemphasized that this invention can be applied similarly and can attain the same function also about a P channel MOS transistor if the point that a conductivity type is mainly reversed polarity is removed.
[0034] Next, the example of an experiment performed in relation to the MOS device concerning the gestalt of this operation is explained.
[0035] (Example of an experiment)
(1) The sample was formed according to the process which carried out the SIMS above-mentioned, and it asked for the profile of each atom of the direction of thickness of a sample according to the secondary ion mass spectrometry (SIMS) by the exposure of primary caesium ion. The result is shown in drawing 6 . As for the sample used for measurement, the polycrystalline silicon layer (220nm) the silicon oxide (10nm) which is gate oxide, acceleration energy 50keV, and 4x1015 doses /are [cm] 2, and are [layer] the gate electrode with which the arsenic was doped, and a titanium silicide layer (70-80nm) are formed on a silicon substrate. And in case this sample is formed, argon ion is poured in with the acceleration energy of 10keV (s) by said process (3).

[0036] It was checked that the peak of an argon is in its layer near the front face of the titanium silicide layer which is the maximum upper layer from drawing 6 .
[0037] (2) The line breadth dependency of the sheet resistance of a gate electrode which the existence of impregnation of argon ion exerts on effect drawing 7 which impregnation of argon ion exerts on the sheet resistance of a gate electrode is compared and shown. In drawing 7 , an axis of abscissa shows the line breadth of the metal silicide layer of a gate electrode, and an axis of ordinate shows the sheet resistance of the gate electrode of electrical-potential-difference 3.3V. Moreover, the sample concerning this invention has the same configuration fundamentally with having used by measurement of the above (1), and two or more sorts of things from which the line breadth of a titanium silicide layer differs were used for it. The sample for a comparison is the same as that of what there is no impregnation of argon ion, and also starts this invention.
[0038] From drawing 7 , by performing amorphous-ization of a gate electrode surface by the ion implantation using argon ion shows that sheet resistance is remarkably small in the range where the line breadth of the titanium silicide layer of a gate electrode is wide compared with the case where argon ion is not poured in. Moreover, when the line breadth of the titanium silicide layer of a gate electrode became small, it was checked that the effectiveness of suppressing the rise of sheet resistance is large.
[0039] (3) The line breadth dependency of the sheet resistance of the source / drain field which the existence of impregnation of argon ion exerts on effect drawing 8 which impregnation of argon ion exerts on the sheet resistance of the source / drain field is compared and shown. In drawing 8 , an axis of abscissa shows the line breadth of the titanium silicide layer of the source / drain field, and an axis of ordinate shows the sheet resistance of the source / drain field of electrical-potential-difference 3.3V. Moreover, the sample concerning this invention has the same configuration fundamentally with what was used by measurement of the above (1), and two or more sorts of things from which the line breadth of a titanium silicide layer differs were used for it. Acceleration energy 50keV and 4x1015 doses /are [cm] 2, and, as for the source / drain field, an arsenic is doped.
[0040] From drawing 8 , by performing amorphous-ization of the source / drain field front face by the ion implantation using argon ion shows that sheet resistance is small in the range where the line breadth of the metal silicide layer of the source / drain field is wide compared with the case where argon ion is not poured in.
[0041] (4) The acceleration energy of argon ion shows the effect which it has on junction leakage current to effect drawing 9 which the acceleration energy of an ion implantation exerts on junction leakage current. In drawing 9 , an axis of abscissa shows the impregnation energy of argon ion, and an axis of ordinate shows the leakage current of electrical-potential-difference 3.3V. The sample used for measurement is the same as that of what was used by measurement of the above (3). Moreover, 41472 micrometers of area of the evaluated area are 2, and the circumference length of area is 864 micrometers.
[0042] the acceleration energy at drawing 9 to the time of an argon ion implantation -- when it becomes large, it turns out that junction leakage current also becomes large. Therefore, as for the acceleration energy at the time of an ion implantation, it is desirable to be set up so that junction leakage current may not exceed a predetermined value. That is, since it is thought that junction leakage current increases when the crystal defect produced by the ion implantation or the defect in which the crystal defect is formed in the process recovered by consecutive heat treatment crosses the source / drain field, as for the acceleration energy at the time of an ion implantation, it is desirable to be set up so that these crystal defects may not cross the source / drain field.
[0043] For example, as shown in drawing 9 , it is possible by setting the acceleration energy at the time of an ion implantation as the suitable range (15 or less keVs) to hold down to the leakage current of the case where argon ion is not being poured in, and this level. However, since the optimum value changes with components, acceleration energy cannot generally limit the value.
[0044] (5) A crystal defect shows the effect which it has on junction leakage current to effect drawing 10 which a crystal defect exerts on junction leakage current. In drawing 10 , an axis of

abscissa shows the thermal wave signal for which it asked by the thermal waving method, and an axis of ordinate shows the junction leak current value of electrical-potential-difference 3.3V. According to the thermal waving method, the quantum of the damage generated in the silicon substrate can be carried out indirectly, and the crystal defect in silicon can be evaluated. The sample of a fundamental configuration used for measurement is the same as that of what was used for measurement of the above (4), and drives it in on the conditions which change an argon with ion implantations. The placing conditions of an argon are as follows.

[0045] a. Dose; the same sign shows [in / 3x1014 pieces // 2, acceleration energy;10keVb. dose;1x1015 piece/cm2, acceleration energy;10keVc. dose;3x1014 piece/cm2, and acceleration energy;30keV drawing 10] the thing corresponding to the placing conditions of the above-mentioned argon cm. In addition, the thermal wave signal shown in the axis of abscissa of drawing 10 measures not using the sample which measured junction leakage current but using the sample which carried out the ion implantation of the argon on above-mentioned a-c and the same conditions at BEASHIRIKON. Moreover, 250000 micrometers of area of the area which evaluated junction leakage current are 2, and the circumference length of area is 2000 micrometers.

[0046] Drawing 10 shows that junction leakage current becomes large as the value of a thermal wave signal becomes large. It shows that junction leakage current becomes large as the crystal defect of this increases.

[0047] (Gestalt of the 2nd operation) Drawing 14 is the sectional view which applied this invention to the CMOS device and in which showing the gestalt of other operations typically, and drawing 11 - drawing 13 are the sectional views showing typically the production process of the semiconductor device shown in drawing 14 .

[0048] The semiconductor device shown in drawing 14 can be manufactured according to the following processes shown in drawing 1111 - drawing 13 .

[0049] (1) Form a twin well by the approach usually used first. That is, the 1st silicon oxide is formed in an oxygen ambient atmosphere on a silicon substrate 101. next, a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. Subsequently, Lynn is poured in using ion-implantation and said photoresist is removed. next, P type -- a well -- in order to form a diffusion layer, a photoresist is applied, patterning is performed using the projection exposing method, and a mask is formed. Subsequently, boron is poured in instead of Lynn using ion-implantation, and said photoresist is removed. then, a thermal diffusion method -- using -- N type -- a well -- diffusion layer 102b and P type -- a well -- diffusion layer 102a is formed.

[0050] Subsequently, after forming a silicon nitride with a CVD method on the 1st silicon oxide, a photoresist is applied, patterning of said photoresist is carried out, and only the part which forms a component isolation region in said 1st silicon oxide removes said silicon nitride in dry etching. Next, after removing said photoresist, the component isolation region 103 which consists of silicon oxide by making a mask oxidize said silicon nitride thermally in an oxygen ambient atmosphere is formed.

[0051] Subsequently, a phosphoric acid etc. removes said silicon nitride, it oxidizes thermally further for the impurity removal on the front face of a substrate before formation of gate oxide, and the 2nd silicon oxide is formed. Then, after etching removes said 2nd silicon oxide, gate oxide 104a and 104b is formed using the oxidizing [thermally] method. Next, a polycrystalline silicon layer is formed using a CVD method, after applying and carrying out patterning of the photoresist, dry etching is performed, gate electrode 105a of an N-channel metal oxide semiconductor transistor and gate electrode 105b of a P channel MOS transistor are formed, and said photoresist is removed.

[0052] Next, in order to carry out short prevention between the gate electrode-source / drain field after silicide, after using a CVD method and forming an oxide film, dry etching is performed and the sidewall spacer 106 is formed. Next, in order to pour in formation of the source / drain field of an N-channel metal oxide semiconductor transistor, and the impurity to the inside of gate electrode 105a, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms an N-channel metal oxide semiconductor

transistor. Next, while pouring in N type impurities, such as an arsenic, with ion-implantation and forming the source / drain fields 107a and 107b which are high-concentration N type diffusion layers, respectively, an impurity is introduced into said gate electrode 105a, and said photoresist is removed after that.
[0053] Similarly, in order to pour in formation of the source / drain field of a P channel MOS transistor, and the impurity to the inside of gate electrode 105b, a photoresist is applied, and patterning is carried out so that opening may be formed in the part equivalent to the field which forms a P channel MOS transistor. Next, while pouring in P type impurities, such as boron, with ion-implantation and forming the source / drain fields 107c and 107d which are high-concentration P type diffusion layers, respectively, an impurity is introduced into said gate electrode 105b, and said photoresist is removed after that. Next, in order to activate the poured-in impurity, it heat-treats in nitrogen-gas-atmosphere mind (drawing 11 R> 1).
[0054] (2) Next, after removing the natural oxidation film which exists in each the gate electrodes 105a and 105b (105), and fields [the source / drain fields / 107a, 107b, 107c, and 107d (107)] front face, in order to make amorphous each front face of said gate electrode 105, and the source / drain field 107, pour in argon ion. The acceleration energy at this time has 15 or less desirable keVs so that the depth of the source / drain field 107 is 0.2 micrometers, and the crystal defect formed with the poured-in argon ion or the crystal defect in which that crystal defect is formed in the process recovered by consecutive heat treatment may not exceed the depth of the source / drain field 107, when performing heat treatment for 20 minutes at 800-900 degrees C after an argon ion implantation. Thus, the amorphous fields 108a and 108c are formed in each front face of the gate electrodes 105a and 105b, and the amorphous fields 108b and 108d are formed in each the source / drain fields 107a and 107b of N-channel metal oxide semiconductor tolan JISHITA, and fields [of P channel MOS tolan JISHITA / the source / drain fields / 107c and 107d] front face (drawing 12 R> 2).
[0055] As mentioned above at this process, it is important for each front face of said gate electrode 105, and the source / drain field 107 by carrying out the ion implantation of the specific ion, such as argon ion, to promote amorphous-ization of silicon. However, it is desirable to make it the crystal defect formed with said specific atomic ion, such as the crystal defect which crosses the source / drain field 107 by this ion implantation, i.e., an argon etc., or the crystal defect in which said crystal defect is formed in the process recovered by consecutive heat treatment not exceed outside said source / drain field 107. consequently, the source / drain field, and a well -- it becomes possible to make it the same level as the case where said ion implantation [leakage current / which is generated by junction to a diffusion layer] aiming at amorphous-izing is not performed. For that purpose, it is desirable to set the acceleration energy at the time of the ion implantation by the atomic ion which does not function as a donor or acceptors, such as argon ion, as conditions on which said crystal defect does not exceed the depth of the impurity diffused layer of the source / drain field.
[0056] And a mask formation process to avoid [for that it is characteristic at this process to be able to perform an ion implantation with a blanket to coincidence, i.e., the whole wafer surface, to the MOS transistor of an N channel and a P channel, since the atomic ion which does not function as a donor or an acceptor, for example, argon ion, is used for the ion implantation for amorphous-izing and] a counter dope is not needed, but it becomes possible to reduce wafer processing cost.
[0057] (3) Next, the metal layer which can form silicide using a spatter, for example, titanium, cobalt, nickel, a tantalum, or platinum, Or form the metal layer 109 which consists of these alloys (drawing 13), and it heat-treats using lamp ANIRA. The metal silicide layers 110a and 110c are formed in each front face of the gate electrodes 105a and 105b. The metal silicide layers 110b and 110d are formed in each the source / drain fields 107a and 107b of N-channel metal oxide semiconductor tolan JISHITA, and fields [of P channel MOS tolan JISHITA / the source / drain fields / 107c and 107d] front face by self-alignment. Subsequently, selectivity etching is performed and the unreacted metal layer on the sidewall spacer 106 and the component isolation region 103 is removed (drawing 14 R> 4).
[0058] As stated above, it also sets in the gestalt of this operation. Like the gestalt of said

operation On each fields [which consist of the gate electrode 105 which consists of polycrystalline silicon before the process (3) which forms the metal layer which can form silicide and N type, or a P type impurity diffused layer / the source / drain fields 107a, 107b, 107c, and 107d] front face By pouring in the specific atomic ion which does not function as a donor or an acceptor by the ion implantation, and having the process (2) which makes said each front face amorphous The reactivity of the silicon which constitutes the source / drain fields 107a, 107b, 107c, and 107d which consist of said gate electrode 105 and N type, or a P type impurity diffused layer can be raised, and silicide-ization can be ensured. Therefore, a good metal silicide layer can be obtained, without affecting the concentration of the impurity of the N type contained to the source / drain field, or P type, while controlling the rise of the sheet resistance of a metal silicide layer, when the width of face of a gate electrode and an impurity diffused layer becomes thin with detailed-izing of a component, and when the depth of said source / drain field becomes small. Moreover, since the ion kind to pour in is the argon which is not the impurity of an arsenic, N type, such as Lynn and BF2, or P type, it does not become a counter dope to the impurity of N type or P type.

[0059] As mentioned above, although this invention was explained based on the gestalt of operation, it cannot be overemphasized that modification various in the range which does not deviate from the summary is possible for this invention, without being limited to the gestalt of the above-mentioned implementation.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 3] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 4] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 5] It is the sectional view showing typically the semiconductor device obtained by the manufacture approach shown in drawing 1 - drawing 4 .
[Drawing 6] It is drawing showing the spectrum of SIMS for which it asked about the sample of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 7] It is drawing for which it asked about the sample of the semiconductor device concerning the gestalt of operation of the 1st of this invention, and the sample for a comparison and in which comparing and showing the relation between the line breadth of the metal silicide layer of a gate electrode, and sheet resistance.
[Drawing 8] It is drawing for which it asked about the sample of the semiconductor device concerning the gestalt of operation of the 1st of this invention, and the sample for a comparison and in which comparing and showing the relation between the line breadth of the metal silicide layer of the source / drain field, and sheet resistance.
[Drawing 9] It is drawing showing the relation between the impregnation energy of argon ion, and junction leakage current.
[Drawing 10] It is drawing showing the relation of the thermal wave signal and junction leakage current which were acquired by the thermal waving method.
[Drawing 11] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 2nd of this invention.
[Drawing 12] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 2nd of this invention.
[Drawing 13] It is the sectional view showing typically one process of the manufacture approach of the semiconductor device concerning the gestalt of operation of the 2nd of this invention.
[Drawing 14] It is the sectional view showing typically the semiconductor device obtained by the manufacture approach shown in drawing 11 - drawing 13 .
[Description of Notations]
101 Silicon Substrate
102 Well -- Diffusion Layer
103 Component Isolation Region
104 Gate Oxide
105 Gate Electrode
106 Sidewall Spacer
107 Source / Drain Field

108 Amorphous Field
109 Metal Layer
110 Metal Silicide Layer

[Translation done.]

* NOTICES *

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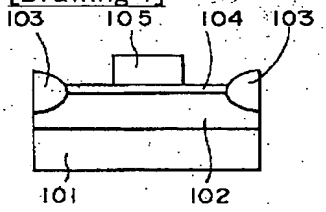
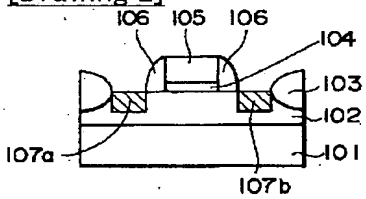
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

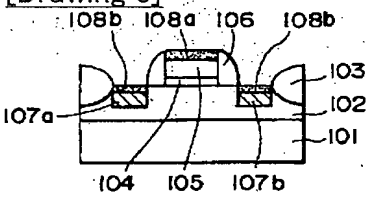
[Drawing 1]



[Drawing 2]



[Drawing 3]



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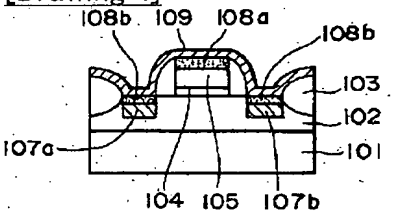

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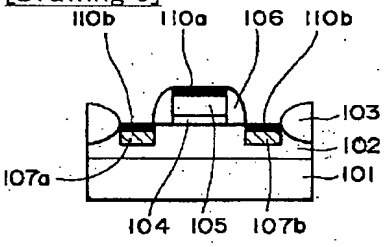
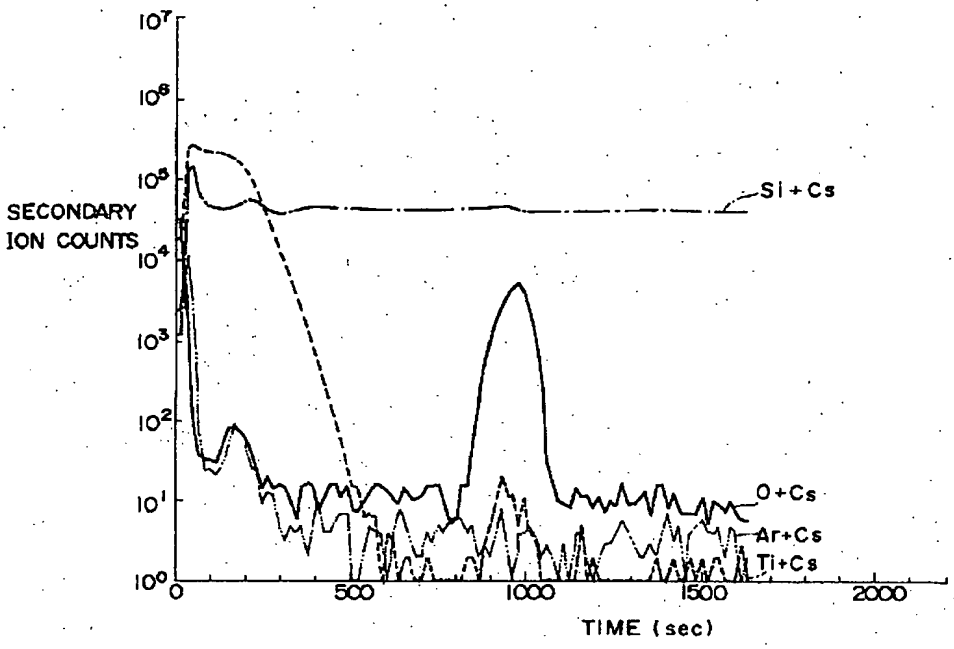
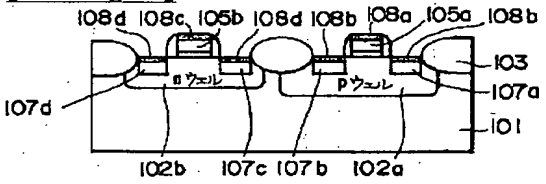


[Drawing 6]



[Drawing 12]



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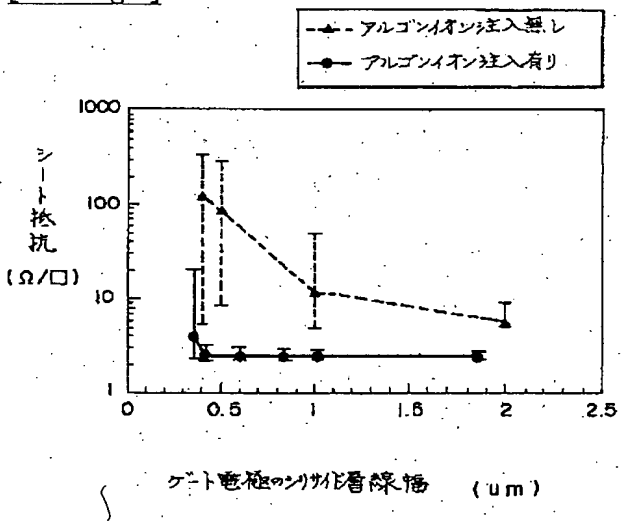
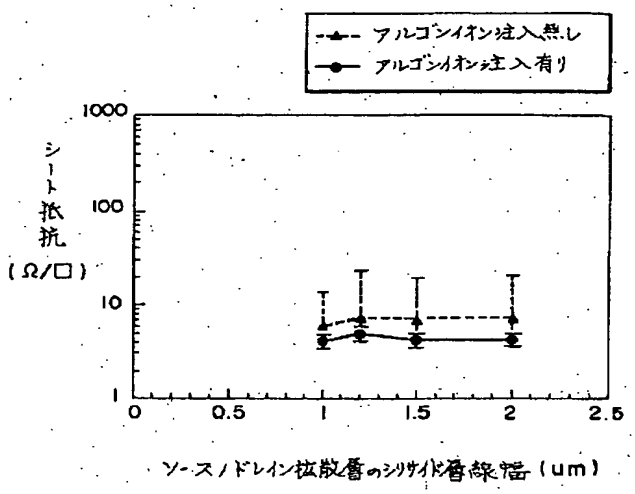
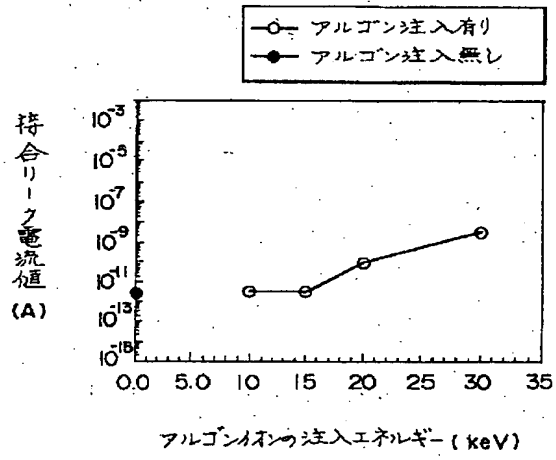


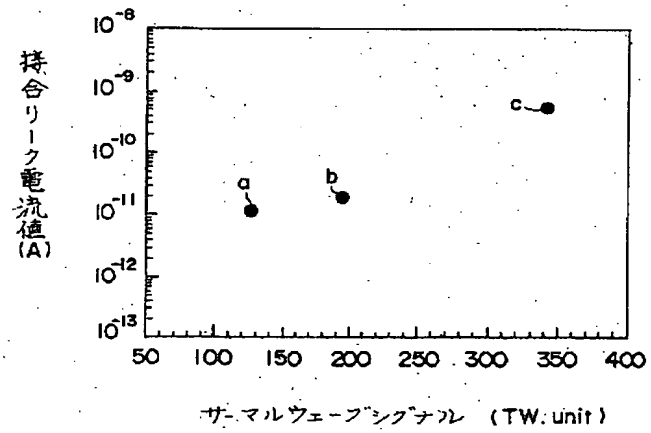
[Drawing 8]



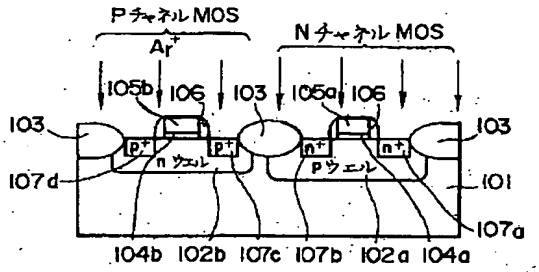
[Drawing 9]



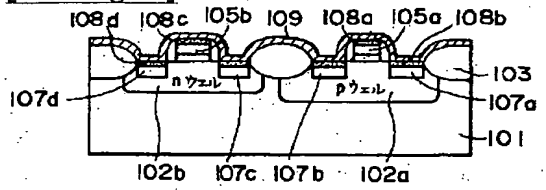
[Drawing 10]



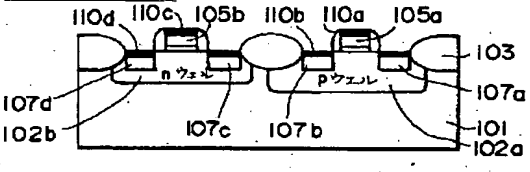
[Drawing 11]



[Drawing 13]



[Drawing 14]



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	21/336				29/78	３０１Ｐ	

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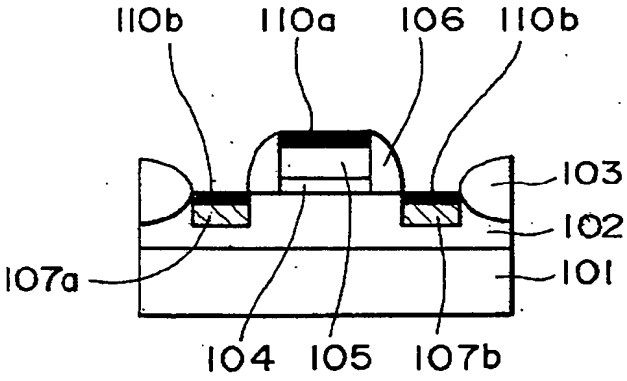
(54)【発明の名称】　ＭＯＳ素子を含む半導体装置およびその製造方法

(57)【要約】　（修正有）

【課題】　ゲート電極とソース／ドレイン領域に金属シリサイド層が形成されたＭＯＳ構造で、製造工程数が増加せず低抵抗金属シリサイド層が得られ、接合リーク電流が抑制される半導体装置とその製造方法を提供する。

【解決手段】　シリコン基板１０１中にＰ型ウエル拡散層１０２、基板上に素子分離領域１０３を形成し、また絶縁膜１０４を介してシリコンを含む導電層からなるゲート電極１０５、及びその両側に側壁スペーサ１０６を形成する。次にウエル拡散層１０２中にＮ型不純物を拡散させ、ソース／ドレイン領域１０７ａ、１０７ｂを形成する。前記導電層１０４及び不純物拡散層１０７の表面にドーパントとして機能しないＡｒやＫｒ原子をイオン注入して該表面を非晶質化する。次に前記表面にＴｉ、Ｎｉ等の高融点金属層１０９をスパッタ法で形成後、熱処理により前記金属層をシリサイド化して所望の半導体装置が得られる。



【特許請求の範囲】
【請求項１】　半導体基板の上に、絶縁膜を介して形成され、少なくともシリコンを含む導電層からなるゲート電極、および、前記半導体基板中に形成され、ソース領域あるいはドレイン領域を構成する不純物拡散層を有し、かつ、前記ゲート電極および前記不純物拡散層は表面に金属シリサイド層を有するＭＯＳ素子を含み、
前記不純物拡散層は、ドナーあるいはアクセプタとなる不純物の他に、イオン注入によって導入された、ドナーあるいはアクセプタとして機能しない原子を含む、ＭＯＳ素子を含む半導体装置。
【請求項２】　請求項１において、
前記ドナーあるいはアクセプタとして機能しない原子は、アルゴン，クリプトン，ネオン，ヘリウムおよびキセノンから選択される希ガスの少なくとも１種、あるいはシリコン，ゲルマニウム，炭素およびスズから選択される少なくとも１種である、ＭＯＳ素子を含む半導体装置。
【請求項３】　請求項１または２において、
前記ドナーあるいはアクセプタとして機能しない原子により形成された結晶欠陥、または前記結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、前記不純物拡散層の中に存在する、ＭＯＳ素子を含む半導体装置。
【請求項４】　半導体基板の上に、絶縁膜を介して形成され、少なくともシリコンを含む導電層からなるゲート電極、および、前記半導体基板中に形成され、ソース領域あるいはドレイン領域を構成する不純物拡散層を有し、かつ、前記ゲート電極および不純物拡散層は表面に金属シリサイド層を有するＭＯＳ素子を含む半導体装置の製造方法であって、
（Ａ）前記半導体基板の上に、絶縁膜を介して、少なくともシリコンを含む導電層を形成する工程、
（Ｂ）前記半導体基板中にドナーあるいはアクセプタとなる不純物を拡散して、ソース領域あるいはドレイン領域を構成する不純物拡散層を形成する工程、
（Ｃ）少なくとも、前記導電層および前記不純物拡散層の表面に、シリサイドを形成しうる金属層を形成する工程、および
（Ｄ）熱処理を行うことにより、前記金属層をシリサイド化する工程、を含み、　前記金属層を形成する工程（Ｃ）より前に、少なくとも、前記導電層および前記不純物拡散層に、イオン注入によってドナーあるいはアクセプタとして機能しない原子を注入する工程を含む、ＭＯＳ素子を含む半導体装置の製造方法。
【請求項５】　請求項４において、
前記ドナーあるいはアクセプタとして機能しない原子は、アルゴン，クリプトン，ネオン，ヘリウムおよびキセノンから選択される希ガスの少なくとも１種、あるいはシリコン，ゲルマニウム，炭素およびスズから選択される少なくとも１種である、ＭＯＳ素子を含む半導体装置の製造方法。
【請求項６】　請求項４または５において、
前記ドナーあるいはアクセプタとして機能しない原子により形成された結晶欠陥、または前記結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、前記不純物拡散層の中に存在する、ＭＯＳ素子を含む半導体装置の製造方法。
【請求項７】　請求項４～６のいずれかにおいて、
前記イオン注入は、ＮチャネルおよびＰチャネルのＭＯＳ素子において、同時に行われる、ＭＯＳ素子を含む半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、サリサイド技術によって形成されたＭＯＳ素子、すなわちゲート電極およびソース／ドレイン領域の表面が金属シリサイド層によって構成されたＭＯＳ素子を含む半導体装置およびその製造方法に関する。
【０００２】
【背景技術および発明が解決しようとする課題】近年、半導体集積回路の更なる高集積化，高性能化をねらい、デバイスの素子寸法は微細化の一途を辿っている。そのため、微細化に伴いＭＯＳトランジスタのソース／ドレイン領域（ソース領域あるいはドレイン領域）を構成する不純物拡散層の幅も狭くなり、またその深さも浅くせざるを得ない状況となっている。しかしながら、ソース／ドレイン領域の深さが浅くなるに従い、不純物拡散層のシート抵抗は上昇し、トランジスタのチャネル抵抗に対し無視できなくなり、その結果、遅延などの点で半導体集積回路の性能を低下させることになる。
【０００３】そのような問題に対して、たとえば文献；電気通信学会　編：ＬＳＩハンドブック、オーム社　p401
にあるように、ソース／ドレイン領域と多結晶シリコンからなるゲート電極の表面をセルフアライメントでシリサイド化する、サリサイド(salicide:self-aligned-silicide)技術が有用である。サリサイド技術を用いることによって、微細化に伴って要求される、ソース／ドレイン領域の低抵抗化をはかることが可能となる。
【０００４】しかしながら、文献；
（１）Robert Beyers et. al. J.Appl. Phys. 61 (11), 1987.
（２）Minoru Takahashi et.al. Ext. Abs. 1993 SSDM, p458
等に開示されているように、ゲート電極およびソース／ドレイン領域に存在する高濃度不純物、特にＮチャネルＭＯＳトランジスタに用いられるヒ素のために、あるいはソース／ドレイン領域およびゲート電極の幅が細くなるといった微細化のために、シリサイド化反応が抑制さ

れ、シート抵抗が上昇してしまうことが知られている。
【０００５】その対策として、シリサイドを形成する前に、ソース／ドレイン領域および多結晶シリコンからなるゲート電極の各表面にヒ素をイオン注入し、シリコンを非晶質化して低抵抗のシリサイドを形成する方法が知られている。
【０００６】この種の方法は、文献；
（１）若林　整　ら、電子情報通信学会技術研究報告　ＳＤＭ９４－１７３
（２）I.Sakai et.al. Digest 1992 Symposium on VLSI Technlgy, p66
等に開示されている。これらの文献に記載された技術においては、トランジスタのソース／ドレイン領域およびゲート電極に導電型半導体にするための不純物を注入，活性化した後、ソース／ドレイン領域およびゲート電極の表面を非晶質化するためにヒ素を注入し、その後シリサイド層を形成するという方法が採られている。
【０００７】しかしながら、先に述べた、非晶質化を目的としてヒ素を打ち込む技術によれば、非晶質化を行うために半導体基板の全面にヒ素をイオン注入すると、前記ヒ素は、例えばホウ素が拡散されたＰ型の不純物層に対してカウンタードープとなってしまい、不純物層のＰ型不純物の濃度を相対的に低下させてしまう。また、それを避けるためには、フォトレジストを用いてパターニングを行い、Ｎ型領域のみにヒ素を打ち込む必要がある。しかし、この方法においては、工程数およびイオン注入時のパターニングに用いるフォトマスクの枚数が増加し、ウエハ加工コストの増大につながる。
【０００８】そこで、本発明は、このような課題を解決しようとするものであり、その目的とするところは、ソース／ドレイン領域およびゲート電極の微細化に伴うシート抵抗の上昇が抑制された、ＭＯＳ素子を含む半導体装置およびその製造方法を提供することにある。
【０００９】
【課題を解決するための手段】本発明に係る、半導体装置の製造方法は、半導体基板の上に、絶縁膜を介して形成され、少なくともシリコンを含む導電層からなるゲート電極、および、前記半導体基板中に形成され、ソース領域あるいはドレイン領域を構成する不純物拡散層を有し、かつ、前記ゲート電極および前記不純物拡散層は表面に金属シリサイド層を有するＭＯＳ素子を含む半導体装置の製造方法であって、（Ａ）前記半導体基板の上に、絶縁膜を介して、少なくともシリコンを含む導電層を形成する工程、（Ｂ）前記半導体基板中にドナーあるいはアクセプタとなる不純物を拡散して、ソース領域あるいはドレイン領域を構成する不純物拡散層を形成する工程、（Ｃ）少なくとも、前記導電層および前記不純物拡散層の表面に、シリサイドを形成しうる金属層を形成する工程、および（Ｄ）熱処理を行うことにより、前記金属層をシリサイド化する工程、を含み、　前記金属層を形成する工程（Ｃ）より前に、少なくとも、前記導電層および前記不純物拡散層に、イオン注入によってドナーあるいはアクセプタとして機能しない原子を注入する工程を含む。
【００１０】本発明の製造方法によって製造された、本発明の半導体装置は、基板の上に、絶縁膜を介して形成され、少なくともシリコンを含む導電層からなるゲート電極、および、前記半導体基板中に形成され、ソース領域あるいはドレイン領域を構成する不純物拡散層を有し、かつ、前記ゲート電極および前記不純物拡散層は表面に金属シリサイド層を有するＭＯＳ素子を含み、前記不純物拡散層は、ドナーあるいはアクセプタとなる不純物の他に、イオン注入によって導入された、ドナーあるいはアクセプタとして機能しない原子を含む。
【００１１】すなわち、本発明の半導体装置は、本発明の製造方法により、シリサイドを形成しうる金属層を形成する工程（Ｃ）より前に、ＭＯＳ素子のゲート電極を構成する導電層、およびソース／ドレイン領域を構成する不純物拡散層の各表面に、ドナーあるいはアクセプタとして機能しない特定の原子イオンをイオン注入によって注入して、前記導電層および不純物拡散層の各表面を非晶質化することにより、前記各層を構成するシリコンの反応性を高め、シリサイド化をより確実に行うことができる。したがって、素子の微細化に伴いゲート電極および不純物拡散層の幅が細くなった場合、ならびに前記不純物拡散層の深さが小さくなった場合においても、金属シリサイド層のシート抵抗の上昇を抑制するとともに、Ｎ型およびＰ型の双方の不純物に対してカウンタードープとならないので、不純物濃度に影響を与えることなく、良好な金属シリサイド層を得ることができる。
【００１２】本発明に係る半導体装置およびその製造方法においては、前記ドナーあるいはアクセプタとして機能しない原子は、アルゴン，クリプトン，ネオン，ヘリウムおよびキセノンから選択される希ガスの少なくとも１種、あるいはシリコン，ゲルマニウム，炭素およびスズから選択される少なくとも１種、好ましくはアルゴンであることが望ましい。
【００１３】これらの原子は、ドナーあるいはアクセプタとして機能しないので、ソース／ドレイン領域に含まれるドナーあるいはアクセプタの濃度に影響を与えることがない。また、これらの原子は、適度な質量を有するのでイオン注入によって被処理層のシリコンを効率よくかつ確実に非晶質化することができる。また、本発明の半導体装置およびその製造方法においては、前記ドナーあるいはアクセプタとして機能しない原子により形成された結晶欠陥、または前記結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、前記不純物拡散層の中に存在する、すなわち前記結晶欠陥がソース／ドレイン領域を構成する不純物拡散層より外側に越えないことが望ましい。その結果、不純物拡散層とウエル

との接合により発生するリーク電流を、非晶質化を目的とした前記イオン注入を行わない場合と同じレベルにすることが可能となる。

【００１４】そのためには、アルゴンイオンなどのドナーあるいはアクセプタとして機能しない原子イオンによる非晶質化を目的とするイオン注入時の加速エネルギーを、イオン注入により生じる結晶欠陥、あるいはその結晶欠陥が後続の熱処理によって回復する工程で形成される結晶欠陥が、ＭＯＳ素子のソース／ドレイン領域の不純物拡散層の深さを越えないような条件にすることが望ましい。

【００１５】また、本発明の製造方法によれば、前述したように、非晶質化のためにイオン注入によって導入される特定の原子は、ソース／ドレイン領域の不純物拡散層の不純物濃度を変化させることがないので、ＮチャネルおよびＰチャネル型のＭＯＳ素子を含む半導体装置の製造において、前記イオン注入は、Ｎ型およびＰ型のＭＯＳ素子において同時に行うことができる。したがって、カウンタドープを避けるためのマスク形成工程を必要とせず、ドナーあるいはアクセプタとして機能しない原子イオンのイオン注入をウエハの全面で行うことができる。

【００１６】以上述べたように、本発明の半導体装置およびその製造方法によれば、アルゴンイオンなどのドナーあるいはアクセプタとして機能しない原子イオンのイオン注入によってシリコンの非晶質化を行うことにより、ソース／ドレイン領域に含まれるＰ型あるいはＮ型の不純物に対してカウンタードープとなることがなく、したがって、前記不純物の濃度を正確にコントロールした状態で、不純物拡散層の良好なシリサイド化が可能である。

【００１７】また、ドナーあるいはアクセプタとして機能しない原子イオンのイオン注入によってシリコンの非晶質化を行うことにより、ソース／ドレイン領域に含まれるＰ型あるいはＮ型の不純物に対してカウンタードープとなることがないので、ウエハ全面において同時にイオン注入することによって、ゲート電極である多結晶シリコン層およびソース／ドレイン領域である単結晶シリコン層の各表面を非晶質化することが可能となるため、フォト工程を追加しイオンを打ち分ける必要がなく、ウエハ加工コストを削減することが可能となる。

【００１８】特に、本発明の半導体装置を携帯機器、たとえば、携帯電話、ノートパソコン、電子手帳、ページャーおよびポケットゲームのようなバッテリー電源駆動の製品に使用した場合、ＭＯＳ素子のシート抵抗を低減するとともに、接合リーク電流を抑制することができ、したがって待機時の電流を小さくでき、電池寿命の延命化がはかることが可能となる。

【００１９】

【発明の実施の形態】以下、本発明の代表的な実施の形態を図面を参照しながら、より詳細に説明する。

【００２０】（第１の実施の形態）図５は、本発明の半導体装置の一例を模式的に示す断面図、図１～図４は、図５に示す半導体装置の製造方法の一例を工程順に模式的に示す断面図である。

【００２１】本実施の形態では、本発明をＮチャネルＭＯＳ素子を含む半導体装置に適用した例を示す。

【００２２】図５に示す半導体装置は、シリコン基板１０１、この基板１０１内に形成されたＰ型ウエル拡散層１０２、前記シリコン基板上に形成された素子分離領域１０３、前記シリコン基板１０１上にゲート酸化膜１０４を介して形成されたゲート電極１０５、このゲート電極１０５の両サイドに形成されたサイドウオールスペーサー１０６、および前記ウエル拡散層１０２中に形成されたＮ型不純物を含むソース／ドレイン領域１０７ａおよび１０７ｂを、含んで構成される。

【００２３】そして、前記ゲート電極１０５は、多結晶シリコンにリンなどのＮ型不純物がドープされて形成され、さらに、このゲート電極１０５の表面には、第１金属シリサイド層１１０ａが形成されている。また、前記ソース／ドレイン領域１０７ａ，１０７ｂの表面には、第２金属シリサイド層１１０ｂが形成されてる。

【００２４】さらに、前記第１および第２金属シリサイド層１１０ａおよび１１０ｂには、イオン注入によって導入された、ドナーあるいはアクセプタとして機能しない原子、たとえばアルゴンが存在する。この原子は、後に詳述するが、シリサイド化を促進するために、前記ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂにイオン注入によってドープされた原子が残ったものである。

【００２５】図５に示す半導体装置は、たとえば図１～図４に示す、以下のプロセスによって製造することができる。

【００２６】（１）まず、シリコン基板１０１上に、酸素雰囲気中で第１シリコン酸化膜を形成する。次にウエル拡散層を形成するためにフォトレジストを塗布し、投影露光法を用いてパターニングを行い、マスクを形成する。ついで、イオン注入法を用いてホウ素を注入し、前記フォトレジストを除去した後、熱拡散法を用いてＰ型ウエル拡散層１０２を形成する。続いてＣＶＤ法でシリコン窒化膜を形成した後フォトレジストを塗布し、前記フォトレジストをパターニングし、前記第１シリコン酸化膜において素子分離領域を形成する部分のみ前記シリコン窒化膜をドライエッチングにて除去する。次に、前記フォトレジストを除去した後、前記シリコン窒化膜をマスクに、酸素雰囲気中で熱酸化させることでシリコン酸化膜からなる素子分離領域１０３を形成する。

【００２７】ついで、リン酸等で前記シリコン窒化膜を除去し、さらにゲート酸化膜の形成前の基板表面の不純物除去のために熱酸化を行い、第２シリコン酸化膜を形

成する。その後、前記第２シリコン酸化膜をエッチングによって除去した後、熱酸化法を用いてゲート酸化膜１０４を形成する。次に、ＣＶＤ法を用いて多結晶シリコン層を形成し、フォトレジストを塗布し、パターニングした後、ドライエッチングを行いゲート電極１０５を形成し、前記フォトレジストを除去する（図１）。

【００２８】（２）次に、シリサイド後のゲート電極－ソース／ドレイン領域間のショートを防止するために、ＣＶＤ法を用いて酸化膜を形成した後、ドライエッチングを行い、サイドウォールスペーサー１０６を形成する。次に、ＮチャネルＭＯＳトランジスタのソース／ドレイン領域の形成、およびゲート電極１０５中への不純物の注入を行うために、フォトレジストを塗布し、ＮチャネルＭＯＳトランジスタを形成する領域に相当する部分に開口部を形成するようにパターニングする。次に、イオン注入法でヒ素などのＮ型不純物を注入し、高濃度のＮ型拡散層であるソース／ドレイン領域１０７ａ，１０７ｂをそれぞれ形成するとともに、前記ゲート電極１０５に不純物を導入し、その後、前記フォトレジストを除去する。次に、注入した不純物の活性化を行うために、窒素雰囲気中で熱処理する（図２）。

【００２９】（３）次に、ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂの各表面に存在する自然酸化膜等を除去した後、ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂの各表面を非晶質化するために、アルゴンイオンを注入する。このときの加速エネルギーは、ソース／ドレイン領域１０７ａ，１０７ｂの深さが、例えば０．２μｍで、アルゴンイオン注入後に８００～９００℃で２０分間の熱処理を行うような場合、注入されたアルゴンイオンにより形成された結晶欠陥、またはその結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、ソース／ドレイン領域１０７ａ，１０７ｂの深さを越えないように、たとえば１５ｋｅＶ以下が望ましい。このようにして、ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂの各表面に非晶質領域１０８ａおよび１０８ｂを形成する（図３）。

【００３０】この工程では、前記ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂの各表面に、アルゴンイオンなどの特定のイオンをイオン注入することによってシリコンの非晶質化を促進することが重要である。ただし、このイオン注入によって、ソース／ドレイン領域を越える結晶欠陥、すなわち、アルゴンなどの前記特定の原子イオンにより形成された結晶欠陥、または前記結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、前記ソース／ドレイン領域１０７ａ，１０７ｂより外側に越えないようにすることが望ましい。その結果、ソース／ドレイン領域とウエル拡散層との接合により発生するリーク電流を、非晶質化を目的とした前記イオン注入を行わない場合と同じレベルにすることが可能となる。そのためには、アルゴンイオンなどのドナーあるいはアクセプタとして機能しない原子イオンによるイオン注入時の加速エネルギーを、前記結晶欠陥がソース／ドレイン領域の不純物拡散層の深さを越えないような条件に設定することが望ましい。

【００３１】（４）次に、スパッタ法を用いてシリサイドを形成しうる金属層、たとえばチタン，コバルト，ニッケル，タンタルまたは白金、あるいはこれらの合金からなる金属層１０９を形成し（図４）、その後ハロゲンランプアニーラーなどのランプアニーラを用いて熱処理を行い、ゲート電極１０５およびソース／ドレイン領域１０７ａ，１０７ｂの表面に金属シリサイド層１１０ａ，１１０ｂをセルフアライメントで形成する。ついで、選択性エッチングを行い、サイドウォールスペーサー１０６および素子分離領域１０３上の未反応金属層を除去する（図５）。

【００３２】以上述べたように、本発明の製造方法においては、シリサイドを形成しうる金属層を形成する工程（４）より前に、多結晶シリコンからなるゲート電極１０５、およびＮ型不純物拡散層からなるソース／ドレイン領域１０７ａ，１０７ｂの各表面に、ドナーあるいはアクセプタとして機能しない特定の原子イオンをイオン注入によって注入して、前記各表面を非晶質化する工程（３）を有することにより、前記ゲート電極１０５、およびＮ型不純物拡散層からなるソース／ドレイン領域１０７ａ，１０７ｂの各層を構成するシリコンの反応性を高め、シリサイド化をより確実に行うことができる。したがって、素子の微細化に伴いゲート電極およびソース／ドレイン領域の幅が細くなった場合、ならびに前記ソース／ドレイン領域の深さが小さくなった場合においても、金属シリサイド層のシート抵抗の上昇を抑制するとともに、Ｎ型不純物、特にシリサイド化を阻害しやすいヒ素を含むソース／ドレイン領域において、不純物濃度に影響を与えることなく、良好な金属シリサイド層を得ることができる。また、注入するイオン種が、ヒ素やリン、BF_2といったＮ型あるいはＰ型の不純物でないアルゴンであるため、他の不純物に対してカウンタードープとなることはない。

【００３３】なお、上記実施の形態においては、ＮチャネルＭＯＳトランジシタについて述べたが、本発明はＰチャネルＭＯＳトランジスタについても、主として導電型が逆極性である点を除けば、同様に適用でき、同様の機能を達成できることはいうまでもない。

【００３４】次に、本実施の形態にかかるＭＯＳ素子に関連して行った実験例について説明する。

【００３５】（実験例）

（１）ＳＩＭＳ

前述したプロセスに準じてサンプルを形成し、セシウム１次イオンの照射による２次イオン質量分析法（ＳＩＭＳ）によって、サンプルの膜厚方向の各原子のプロファ

イルを求めた。その結果を図6に示す。測定に用いたサンプルは、シリコン基板上に、ゲート酸化膜であるシリコン酸化膜（10nm）、加速エネルギー50keV、およびドーズ量が4×10^{15}個／cm^2で、ヒ素がドーピングされたゲート電極である多結晶シリコン層（220nm）、およびチタンシリサイド層（70～80nm）が形成されたものである。そして、このサンプルを形成する際には、前記工程（3）で、アルゴンイオンが10keVの加速エネルギーで注入されている。

【0036】図6から、最上層であるチタンシリサイド層の表面近傍およびその層中に、アルゴンのピークがあることが確認された。

【0037】（2）アルゴンイオンの注入がゲート電極のシート抵抗に及ぼす影響

図7に、アルゴンイオンの注入の有無が及ぼす、ゲート電極のシート抵抗の線幅依存性を比較して示す。図7において、横軸はゲート電極の金属シリサイド層の線幅を示し、縦軸は電圧3．3Vでのゲート電極のシート抵抗を示す。また、本発明に係るサンプルは、上記（1）の測定で用いたと基本的に同様の構成を有し、チタンシリサイド層の線幅が異なるものを複数種用いた。比較用のサンプルは、アルゴンイオンの注入がない他は、本発明にかかるものと同様である。

【0038】図7から、アルゴンイオンを用いたイオン注入によってゲート電極表面の非晶質化を行うことにより、アルゴンイオンの注入を行わない場合に比べて、ゲート電極のチタンシリサイド層の線幅の広い範囲においてシート抵抗が著しく小さいことがわかる。また、ゲート電極のチタンシリサイド層の線幅が小さくなった場合においても、シート抵抗の上昇を抑える効果が大きいことが確認された。

【0039】（3）アルゴンイオンの注入がソース／ドレイン領域のシート抵抗に及ぼす影響

図8に、アルゴンイオンの注入の有無が及ぼす、ソース／ドレイン領域のシート抵抗の線幅依存性を比較して示す。図8において、横軸はソース／ドレイン領域のチタンシリサイド層の線幅を示し、縦軸は電圧3．3Vでのソース／ドレイン領域のシート抵抗を示す。また、本発明に係るサンプルは、上記（1）の測定で用いたものと基本的に同様の構成を有し、チタンシリサイド層の線幅が異なるものを複数種用いた。ソース／ドレイン領域は、加速エネルギー50keV、およびドーズ量が4×10^{15}個／cm^2で、ヒ素がドーピングされたものである。

【0040】図8から、アルゴンイオンを用いたイオン注入によってソース／ドレイン領域表面の非晶質化を行うことにより、アルゴンイオンの注入を行わない場合に比べて、ソース／ドレイン領域の金属シリサイド層の線幅の広い範囲においてシート抵抗が小さいことがわかる。

【0041】（4）イオン注入の加速エネルギーが接合リーク電流に及ぼす影響

図9に、アルゴンイオンの加速エネルギーが接合リーク電流に与える影響を示す。図9において、横軸はアルゴンイオンの注入エネルギーを示し、縦軸は電圧3．3Vでのリーク電流を示す。測定に用いたサンプルは、上記（3）の測定で用いたものと同様である。また、評価したエリアの面積は$41472\mu m^2$であり、エリアの周辺長は$864\mu m$である。

【0042】図9から、アルゴンイオン注入時の加速エネルギー大きくなると、接合リーク電流も大きくなることがわかる。したがって、イオン注入時の加速エネルギーは、接合リーク電流が所定の値を越えないように設定されることが望ましい。すなわち、接合リーク電流は、イオン注入により生じる結晶欠陥、あるいはその結晶欠陥が後続の熱処理によって回復する過程で形成される欠陥が、ソース／ドレイン領域を越えることによって増大すると考えられるので、イオン注入時の加速エネルギーは、これらの結晶欠陥がソース／ドレイン領域を越えないように設定されることが望ましい。

【0043】たとえば、図9に示すように、イオン注入時の加速エネルギーを適切な範囲（15keV以下）に設定することによって、アルゴンイオンを注入していない場合と同レベルのリーク電流に抑えることが可能である。ただし、加速エネルギーは、素子によってその最適値が異なるので、一概にその値を限定することはできない。

【0044】（5）結晶欠陥が接合リーク電流に及ぼす影響

図10に、結晶欠陥が接合リーク電流に与える影響を示す。図10において、横軸はサーマルウエーブ法によって求めたサーマルウエーブシグナルを示し、縦軸は電圧3．3Vでの接合リーク電流値を示す。サーマルウエーブ法によれば、シリコン基板中に発生したダメージを間接的に定量でき、シリコン中の結晶欠陥を評価することができる。測定に用いたサンプルは、基本的構成は上記（4）の測定に用いたものと同様であり、イオン注入によってアルゴンを異なる条件で打ち込んだものである。アルゴンの打ち込み条件は以下の通りである。

【0045】a．ドーズ量；3×10^{14}個／cm^2，加速エネルギー；10keV

b．ドーズ量；1×10^{15}個／cm^2，加速エネルギー；10keV

c．ドーズ量；3×10^{14}個／cm^2，加速エネルギー；30keV

図10において、上記アルゴンの打ち込み条件に対応するものを同じ符号で示す。なお、図10の横軸に示されるサーマルウエーブシグナルは、接合リーク電流を測定したサンプルではなく、ベアシリコンに上記a～cと同じ条件でアルゴンをイオン注入したサンプルを用いて測

定したものである。また、接合リーク電流を評価したエリアの面積は２５００００μm²であり、エリアの周辺長は２０００μmである。

【００４６】図１０から、サーマルウエーブシグナルの値が大きくなるにつれて、接合リーク電流が大きくなることがわかる。このことは、結晶欠陥が多くなるに従って接合リーク電流が大きくなることを示している。

【００４７】（第２の実施の形態）図１４は、本発明をＣＭＯＳ素子に適用した、他の実施の形態を模式的に示す断面図であり、図１１～図１３は、図１４に示す半導体装置の製造工程を模式的に示す断面図である。

【００４８】図１４に示す半導体装置は、たとえば、図１１～図１３に示す、以下のプロセスによって製造することができる。

【００４９】（１）まず、通常用いられる方法によってツインウェルを形成する。すなわち、シリコン基板１０１上に、酸素雰囲気中で第１シリコン酸化膜を形成する。次にウエル拡散層を形成するためにフォトレジストを塗布し、投影露光法を用いてパターニングを行い、マスクを形成する。ついで、イオン注入法を用いてリンを注入し、前記フォトレジストを除去する。次に、Ｐ型ウエル拡散層を形成するためにフォトレジストを塗布し、投影露光法を用いてパターニングを行い、マスクを形成する。ついで、イオン注入法を用いてリンの代わりにホウ素を注入し、前記フォトレジストを除去する。その後、熱拡散法を用いてＮ型ウエル拡散層１０２ｂおよびＰ型ウエル拡散層１０２ａを形成する。

【００５０】次いで、第１シリコン酸化膜上に、ＣＶＤ法でシリコン窒化膜を形成した後フォトレジストを塗布し、前記フォトレジストをパターニングし、前記第１シリコン酸化膜において素子分離領域を形成する部分のみ前記シリコン窒化膜をドライエッチングにて除去する。次に、前記フォトレジストを除去した後、前記シリコン窒化膜をマスクに、酸素雰囲気中で熱酸化させることでシリコン酸化膜からなる素子分離領域１０３を形成する。

【００５１】ついで、リン酸等で前記シリコン窒化膜を除去し、さらにゲート酸化膜の形成前の基板表面の不純物除去のために熱酸化を行い、第２シリコン酸化膜を形成する。その後、前記第２シリコン酸化膜をエッチングによって除去した後、熱酸化法を用いてゲート酸化膜１０４ａ，１０４ｂを形成する。次に、ＣＶＤ法を用いて多結晶シリコン層を形成し、フォトレジストを塗布し、パターニングした後、ドライエッチングを行い、ＮチャネルＭＯＳトランジスタのゲート電極１０５ａおよびＰチャネルＭＯＳトランジスタのゲート電極１０５ｂを形成し、前記フォトレジストを除去する。

【００５２】次に、シリサイド後のゲート電極ーソース／ドレイン領域間のショート防止するために、ＣＶＤ法を用いて酸化膜を形成した後、ドライエッチングを行いサイドウォールスペーサー１０６を形成する。次に、ＮチャネルＭＯＳトランジスタのソース／ドレイン領域の形成、およびゲート電極１０５ａ中への不純物の注入を行うために、フォトレジストを塗布し、ＮチャネルＭＯＳトランジスタを形成する領域に相当する部分に開口部を形成するようにパターニングする。次に、イオン注入法でヒ素などのＮ型不純物を注入し、高濃度のＮ型拡散層であるソース／ドレイン領域１０７ａ，１０７ｂをそれぞれ形成するとともに、前記ゲート電極１０５ａに不純物を導入し、その後、前記フォトレジストを除去する。

【００５３】同様に、ＰチャネルＭＯＳトランジスタのソース／ドレイン領域の形成、およびゲート電極１０５ｂ中への不純物の注入を行うために、フォトレジストを塗布し、ＰチャネルＭＯＳトランジスタを形成する領域に相当する部分に開口部を形成するようにパターニングする。次に、イオン注入法でホウ素などのＰ型不純物を注入し、高濃度のＰ型拡散層であるソース／ドレイン領域１０７ｃ，１０７ｄをそれぞれ形成するとともに、前記ゲート電極１０５ｂに不純物を導入し、その後、前記フォトレジストを除去する。次に、注入した不純物の活性化を行うために、窒素雰囲気中で熱処理する（図１１）。

【００５４】（２）次に、ゲート電極１０５ａ，１０５ｂ（１０５）およびソース／ドレイン領域１０７ａ，１０７ｂ，１０７ｃ，１０７ｄ（１０７）の各表面に存在する自然酸化膜等を除去した後、前記ゲート電極１０５およびソース／ドレイン領域１０７の各表面を非晶質化するために、アルゴンイオンを注入する。このときの加速エネルギーは、ソース／ドレイン領域１０７の深さが、例えば０．２μmで、アルゴンイオン注入後に８００～９００℃で２０分間の熱処理を行うような場合、注入されたアルゴンイオンにより形成された結晶欠陥、またはその結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、ソース／ドレイン領域１０７の深さを越えないように、たとえば１５ｋｅＶ以下が望ましい。このようにして、ゲート電極１０５ａ，１０５ｂの各表面に非晶質領域１０８ａ，１０８ｃを形成し、ＮチャネルＭＯＳトランジシタのソース／ドレイン領域１０７ａ，１０７ｂおよびＰチャネルＭＯＳトランジシタのソース／ドレイン領域１０７ｃ，１０７ｄの各表面に非晶質領域１０８ｂおよび１０８ｄを形成する（図１２）。

【００５５】この工程では、前述したように、前記ゲート電極１０５およびソース／ドレイン領域１０７の各表面に、アルゴンイオンなどの特定のイオンをイオン注入することによってシリコンの非晶質化を促進することが重要である。ただし、このイオン注入によって、ソース／ドレイン領域１０７を越える結晶欠陥、すなわち、アルゴンなどの前記特定の原子イオンにより形成された結

晶欠陥、または前記結晶欠陥が後続の熱処理によって回復する過程で形成される結晶欠陥が、前記ソース／ドレイン領域１０７より外側に越えないようにすることが望ましい。その結果、ソース／ドレイン領域とウエル拡散層との接合により発生するリーク電流を、非晶質化を目的とした前記イオン注入を行わない場合と同じレベルにすることが可能となる。そのためには、アルゴンイオンなどのドナーあるいはアクセプタとして機能しない原子イオンによるイオン注入時の加速エネルギーを、前記結晶欠陥がソース／ドレイン領域の不純物拡散層の深さを越えないような条件に設定することが望ましい。

【００５６】そして、この工程で特徴的なことは、非晶質化のためのイオン注入にはドナーあるいはアクセプタとして機能しない原子イオン、たとえばアルゴンイオンが用いられるため、ＮチャネルおよびＰチャネルのＭＯＳトランジスタに対して同時に、つまりウエハ全面に対してブランケットにイオン注入を行うことができ、カウンタドープを避けるためのマスク形成工程を必要とせず、ウエハ加工コストを削減することが可能となる。

【００５７】（３）次に、スパッタ法を用いてシリサイドを形成しうる金属層、たとえばチタン，コバルト，ニッケル，タンタルまたは白金、あるいはこれらの合金からなる金属層１０９を形成し（図１３）、ランプアニーラーを用いて熱処理を行い、ゲート電極１０５ａ，１０５ｂの各表面に金属シリサイド層１１０ａ，１１０ｃを形成し、ＮチャネルＭＯＳトランジシタのソース／ドレイン領域１０７ａ，１０７ｂおよびＰチャネルＭＯＳトランジシタのソース／ドレイン領域１０７ｃ，１０７ｄの各表面に金属シリサイド層１１０ｂおよび１１０ｄをセルフアライメントで形成する。ついで、選択性エッチングを行い、サイドウォールスペーサー１０６および素子分離領域１０３上の未反応金属層を除去する（図１４）。

【００５８】以上述べたように、本実施の形態においても、前記実施の形態と同様に、シリサイドを形成しうる金属層を形成する工程（３）より前に、多結晶シリコンからなるゲート電極１０５、およびＮ型またはＰ型不純物拡散層からなるソース／ドレイン領域１０７ａ，１０７ｂ，１０７ｃ，１０７ｄの各表面に、ドナーあるいはアクセプタとして機能しない特定の原子イオンをイオン注入によって注入して、前記各表面を非晶質化する工程（２）を有することにより、前記ゲート電極１０５、およびＮ型またはＰ型不純物拡散層からなるソース／ドレイン領域１０７ａ，１０７ｂ，１０７ｃ，１０７ｄを構成するシリコンの反応性を高め、シリサイド化をより確実に行うことができる。したがって、素子の微細化に伴いゲート電極および不純物拡散層の幅が細くなった場合、ならびに前記ソース／ドレイン領域の深さが小さくなった場合においても、金属シリサイド層のシート抵抗の上昇を抑制するとともに、ソース／ドレイン領域に含まれるＮ型またはＰ型の不純物の濃度に影響を与えることなく、良好な金属シリサイド層を得ることができる。また、注入するイオン種が、ヒ素やリン、BF_2といったＮ型あるいはＰ型の不純物でないアルゴンなどであるため、Ｎ型あるいはＰ型の不純物に対してカウンタードープとなることはない。

【００５９】以上、本発明を実施の形態に基づいて説明したが、本発明は上記実施の形態に限定されることなく、その要旨を逸脱しない範囲で種々の変更が可能であることは言うまでもない。

【００６０】

【図面の簡単な説明】

【図１】本発明の第１の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図２】本発明の第１の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図３】本発明の第１の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図４】本発明の第１の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図５】図１～図４に示す製造方法によって得られた半導体装置を模式的に示す断面図である。

【図６】本発明の第１の実施の形態にかかる半導体装置のサンプルについて求めたＳＩＭＳのスペクトルを示す図である。

【図７】本発明の第１の実施の形態にかかる半導体装置のサンプルおよび比較用のサンプルについて求めた、ゲート電極の金属シリサイド層の線幅とシート抵抗との関係を比較して示す図である。

【図８】本発明の第１の実施の形態にかかる半導体装置のサンプルおよび比較用のサンプルについて求めた、ソース／ドレイン領域の金属シリサイド層の線幅とシート抵抗との関係を比較して示す図である。

【図９】アルゴンイオンの注入エネルギーと接合リーク電流との関係を示す図である。

【図１０】サーマルウエーブ法によって得られたサーマルウエーブシグナルと接合リーク電流との関係を示す図である。

【図１１】本発明の第２の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図１２】本発明の第２の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

【図１３】本発明の第２の実施の形態にかかる半導体装置の製造方法の一工程を模式的に示す断面図である。

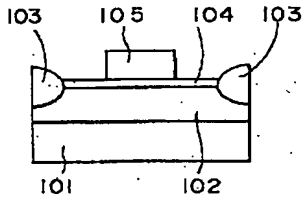
【図１４】図１１～図１３に示す製造方法によって得られた半導体装置を模式的に示す断面図である。

【符号の説明】

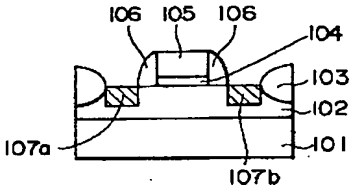
１０１　シリコン基板
１０２　ウエル拡散層
１０３　素子分離領域

１０４　ゲート酸化膜
１０５　ゲート電極
１０６　サイドウォールスペーサー
１０７　ソース／ドレイン領域
１０８　非晶質領域
１０９　金属層
１１０　金属シリサイド層

【図１】



【図２】



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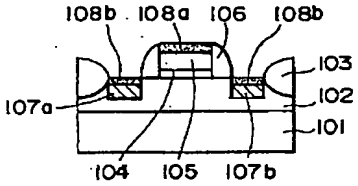

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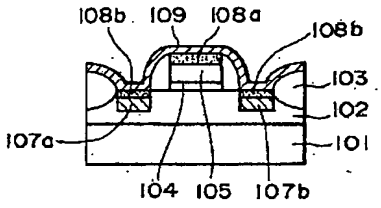

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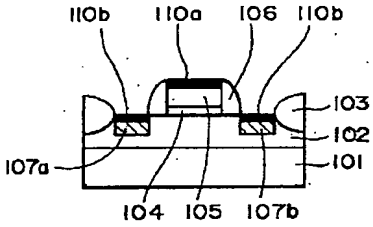
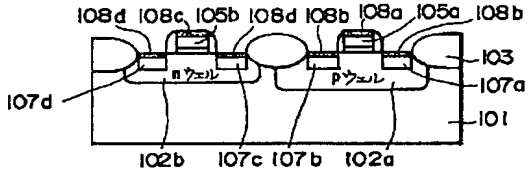
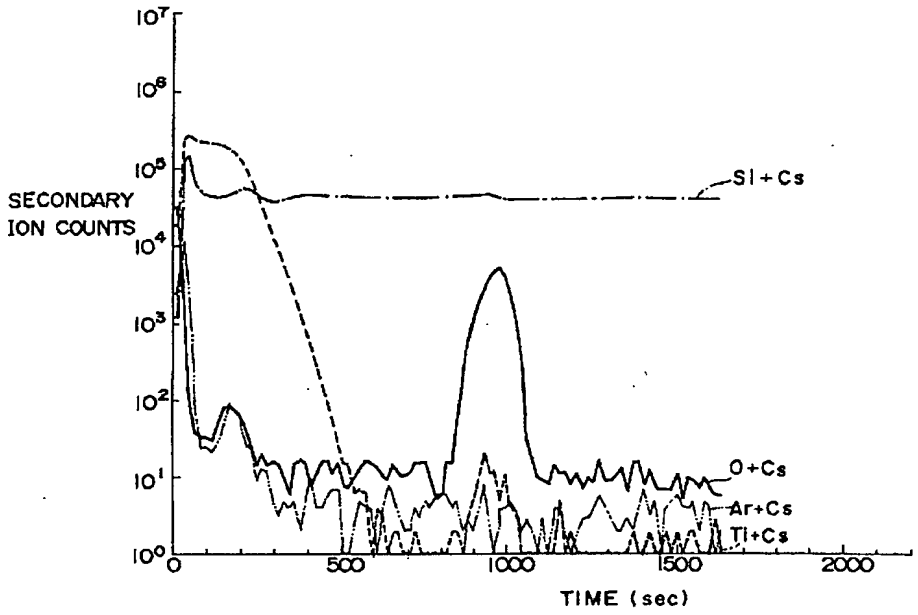


【図１２】



【図６】



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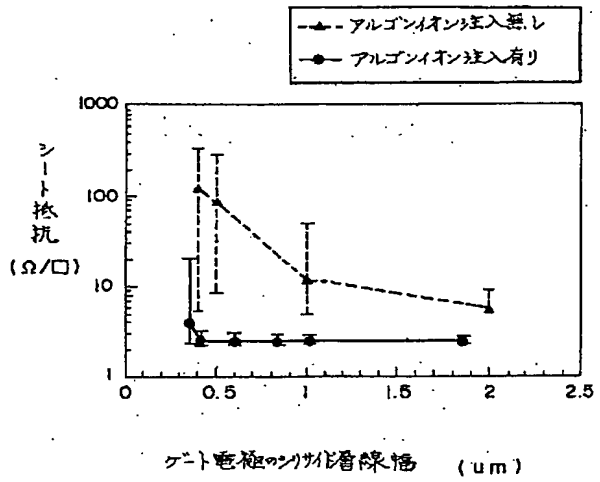

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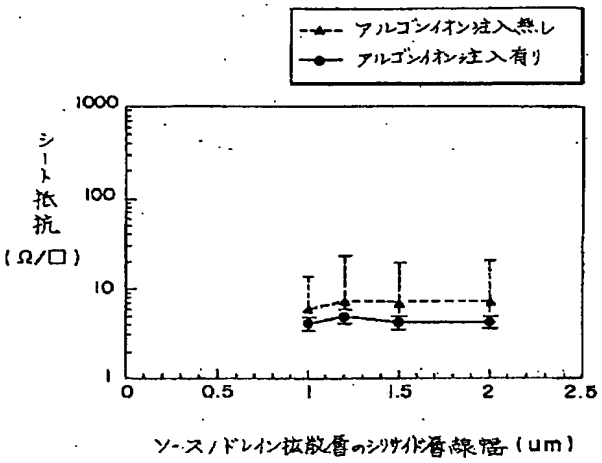

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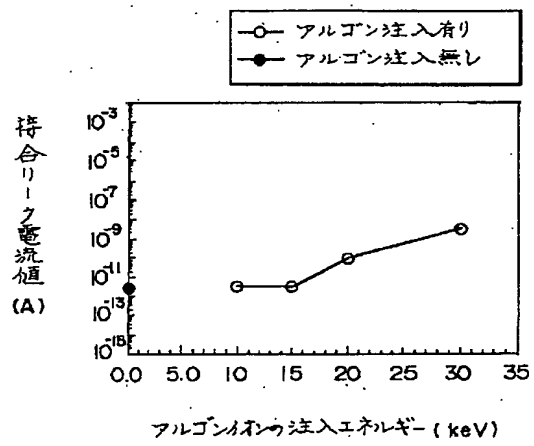
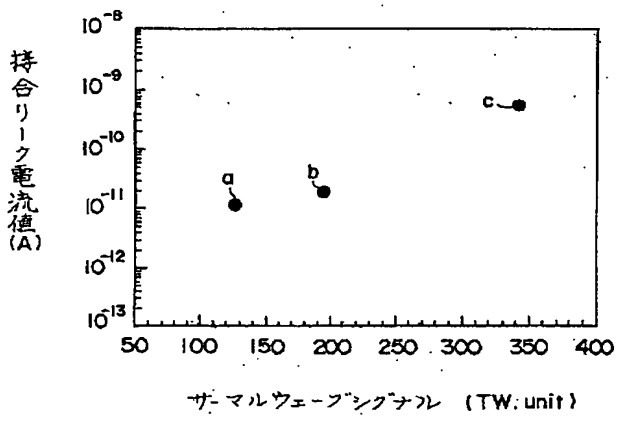
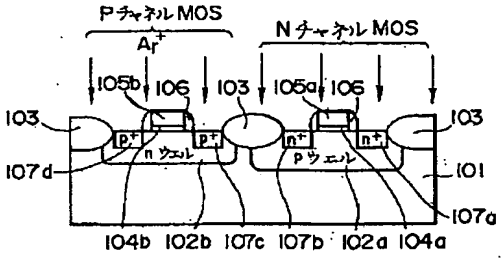


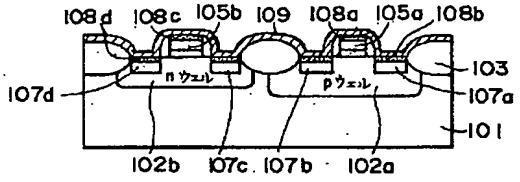
【図１０】



【図１１】



【図１３】



【図１４】